

L-Band Radar Transistor

The high power pulsed radar transistor device part number IB1214M55 is designed for L-Band radar systems operating over the instantaneous bandwidth of 1.215-1.400 GHz. While operating in class C mode this common base device supplies a minimum of 55 watts of peak pulse power under the conditions of 100 μ s pulse width and 10% duty cycle. All devices are 100% screened for large signal RF parameters.



Silicon Bipolar

- Ultra-high f_T

Class C Operation

- High Efficiency

Common Base Configuration

- Single Power Supply

Gold Metal

- Maximum Reliability

Emitter Ballasting

- Optimum Thermal Distribution

Internal Impedance Matching

- Ease of Use
- Ultra-low Loss Design

Be0 Package

- Unmatched Thermal Reliability

RF Test Fixture

- Broadband
- Matched to 50 Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

General Information	Test Sequence	Freq	PIN	RL	POUT	GP	dG	IC	nc	Droop	VSWR-S	VSWR-LMT	
IB1214M55	Name	(MHz)	(W)	(dB)	(W)	(dB)	(dB)	(A)	(%)	(dB)	1.5:1 (P-F)	2:1 (P-F)	
Date:	4/7/2009												
Assbly Lot - SN :	D2530-5	Nominal	1215	6.0	-12.0	55	9.62	2.370	58.0	0.00	P	P	
Wafer :	NA												
Test Fixture :	414	Nominal	1300	6.3	-13.0	55	9.41	1.03	2.390	57.5	0.10	P	P
Pass / Fail :	Device Passes												
OPERATOR:	FB	Nominal	1400	7.6	-14.0	55	8.60	2.900	47.4	0.10	P	P	
Pulse: 100us-10%	Vcc=40V												

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Collector-Emitter Voltage	V_{CES}	--	75	V	$V_{BE}=0V$.
BD	Emitter-Base Voltage	V_{EBO}	--	2	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-40	+150	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.62	°C/W	$V_{CC}=40V$, Pulse Format=100us, 10%, $T_F=25\pm 5^\circ C$, $P_{in}=8.7W$, $P_{out}=55W$, $N_C=40\%$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification.
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C.
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

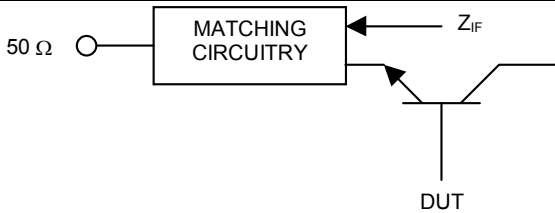
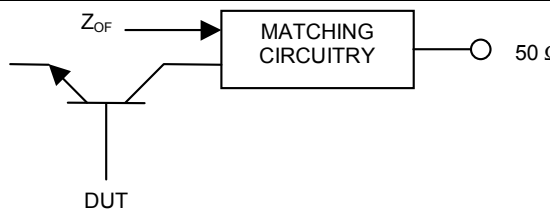
DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Collector-Emitter Breakdown Voltage	BV_{CES}	75	--	V	$I_C=10mA$, $V_{BE}=0V$, $T_F=25\pm 5^\circ C$.
100%	Zero Base Voltage Collector Leakage Current	I_{CES}	--	5.0	mA	$V_{CE}=40V$, $V_{BE}=0V$, $T_F=25\pm 5^\circ C$.
100%	DC Current Gain	H_{FE}	20	120	--	$V_{CE}=5V$, $I_C=0.1A$, $T_F=25\pm 5^\circ C$.

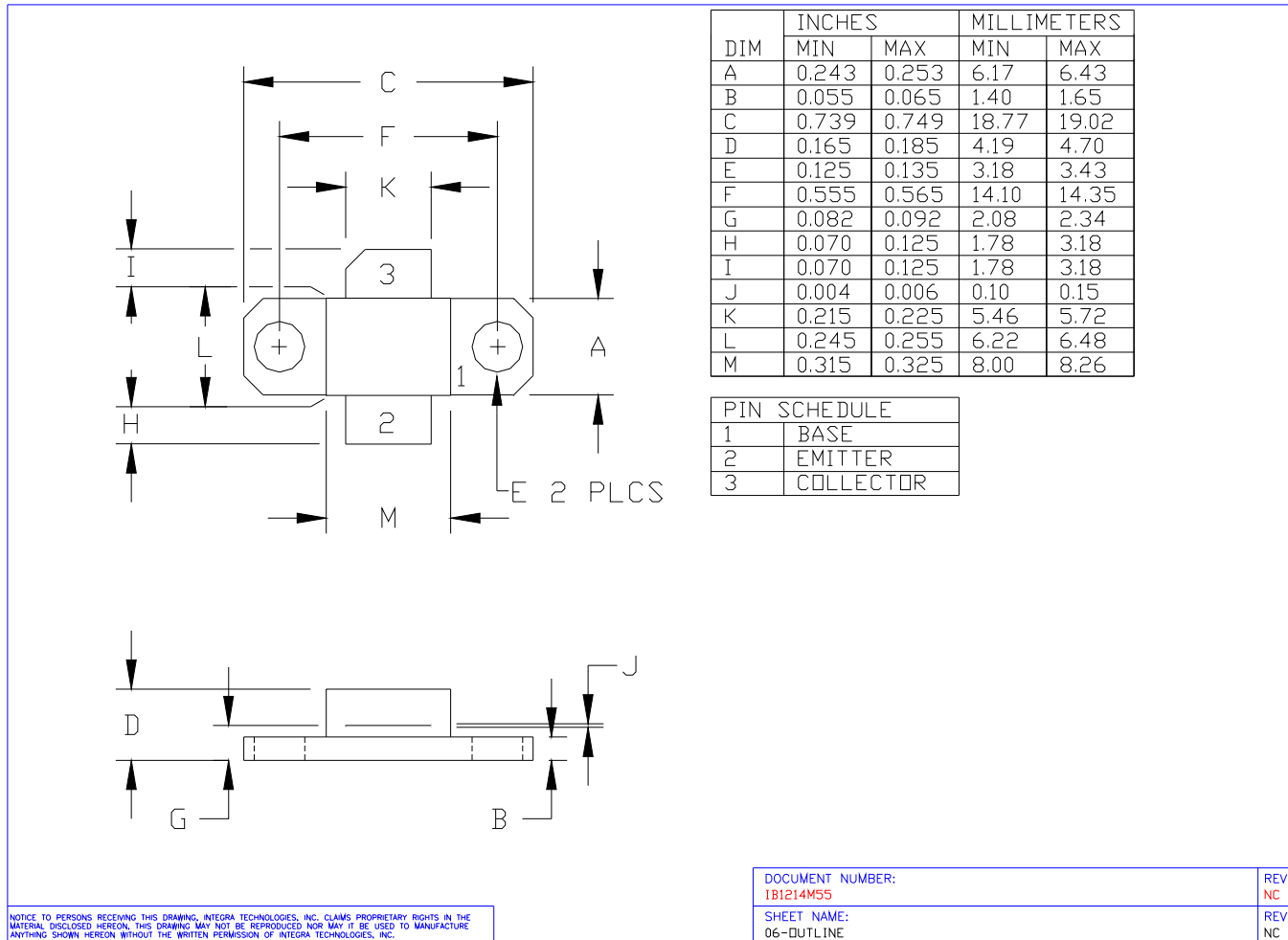
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-8	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=P_{OUT1}, P_{OUT2}, P_{OUT3}, F=F1, F2, F3.$
100%	Input Power	P_{IN}	3.5	8.7	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=P_{OUT1}, P_{OUT2}, P_{OUT3}, F=F1, F2, F3.$
100%	Power Gain	G_p	8.0	12.0	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=P_{OUT1}, P_{OUT2}, P_{OUT3}, F=F1, F2, F3.$
100%	Collector Efficiency ($P_o/I_c/V_{CC}$)	N_C	40	75	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=P_{OUT1}, P_{OUT2}, P_{OUT3}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	Droop	-0.5	0.5	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=P_{OUT1}, P_{OUT2}, P_{OUT3}, F=F1, F2, F3.$
100%	Stability into 1.5:1 VSWR with +0.75dB overdrive	VSWR-S	--	--	--	Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
100%	2:1 Load Mismatch Tolerance	VSWR-LMT	--	--	--	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=P_{OUT1}, P_{OUT2}, P_{OUT3}, F=F1, F2, F3.$ Rotate 2:1 output VSWR through 360° phase. Post test P_o = Pre test $P_o \pm 10W$.
Note	$V1 = 40V; PW1 = 100\mu s; DF1 = 10%; P_{OUT1} = P_{OUT2} = P_{OUT3} = 55W; F1 = 1.215 GHz, F2 = 1.300 GHz, F3 = 1.400 GHz.$					
Note	T_F = Device flange temperature.					
Note	Screen 'BD' = parameter qualified By Design.					

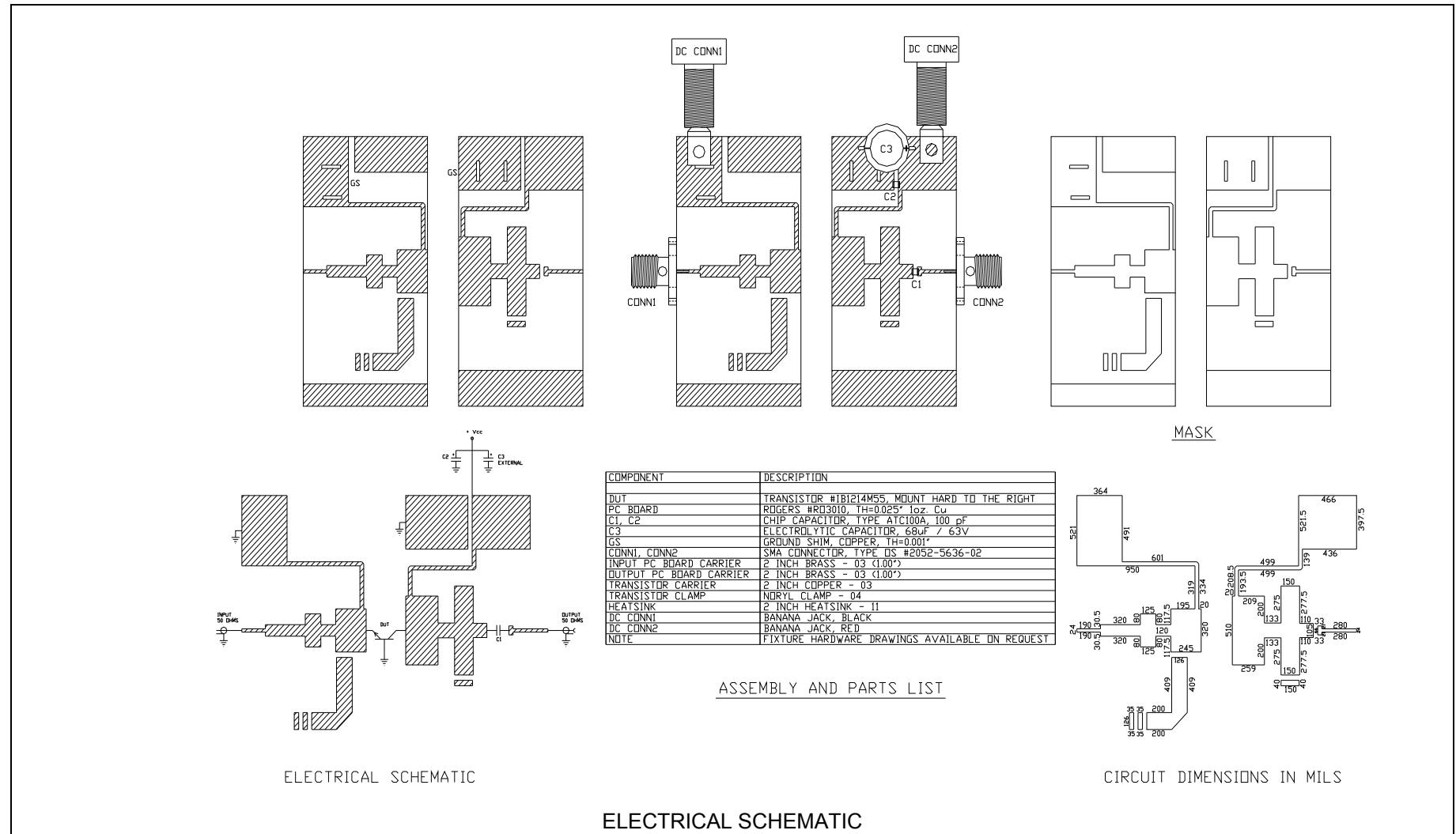
BROADBAND RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (MHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
1.215	2.88 - j2.3	1.5 + j1.05
1.300	3 - j1.6	1.7 + j2.1
1.400	3.38 - j0.89	2.11 + j3.65
Impedance Definition		

PACKAGE DIMENSIONAL OUTLINE DRAWING



RF TEST FIXTURE



DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

DISCLAIMER

Integra Technologies Inc. reserves the right to make changes without further notice to any products herein. Integra Technologies Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Integra Technologies Inc. assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Integra Technologies Inc. products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integra Technologies Inc. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integra Technologies Inc. for any damages resulting from such improper use or sale.
--