

Part Number: **IGN0912L500 (Preliminary)**



L-Band Avionics Transistor

IGN0912L500 is an internally pre-matched, gallium nitride (GaN) high electron mobility transistor (HEMT). This part is designed for L-Band avionics applications operating over the 960 – 1215 MHz instantaneous frequency band. Under 444x(7 μ s ON, 6 μ s OFF), 22.7% pulse conditions it supplies a minimum of 500 watts of peak output power with 17dB minimum gain. Specified operation is with Class AB bias. When appropriately rated, it is operable under a wide range of pulse widths and duty factors. All devices are 100% screened for large parameter RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. Not recommended for CW operation.



TECHNOLOGIES, INC.

GaN on Silicon Carbide FET

- High Power Gain
- Excellent thermal stability
- Gold Metal

Depletion Mode Device

- Negative Gate Voltage to Bias
- Bias Sequencing Required
- See App Note to Prevent Damage

Gold Metal System

- Complete Gold System
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

Class AB Operation

- Specified with AB bias

Internal Impedance Matching

- Ease of Use
- Ultra Low Loss Design

BeO Free Package

- Metal Based
- Epoxy Seal

High Power RF Test / Fixture

- Broadband
- Matched to 50 Ω (ohms)
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

PRELIMINARY RF DATA

PRELIMINARY RF DATA

Lot/SN	F (MHz)	Pi (W)	Id (A)	RL (dB)	Po (W)	Nd (%)	G (dB)	Drp (dB)	VSWR	
									2:1	3:1
50094123-1	960	9	17.665	10	594	67.3	18.20	-0.25	S	P
	1090	9	17.269	11	563	65.2	17.96	-0.28	S	P
	1215	9	17.401	12	541	62.2	17.79	-0.34	S	P

Vd=50V, IdQ=250mA, 444x(7 μ s ON, 6 μ s OFF), 22.7%

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	60	V	--
BD	Gate-Source Voltage	V_{GS}	-10	0	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
BD	CW operation	--	--	--	--	Not rated for CW operation
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	TBD	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=500W$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					


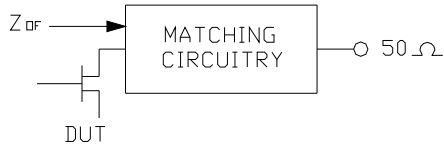
DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Drain Leakage	I_{D-OFF}	--	21	--	mA	$V_G = -8V, V_D = 50V, T_F = 25\pm5^\circ C$
100%	Threshold Voltage	V_{GS-TH}	--	-2.8	--	V	$V_D = 50V, I_D = 250mA, T_F = 25\pm5^\circ C$

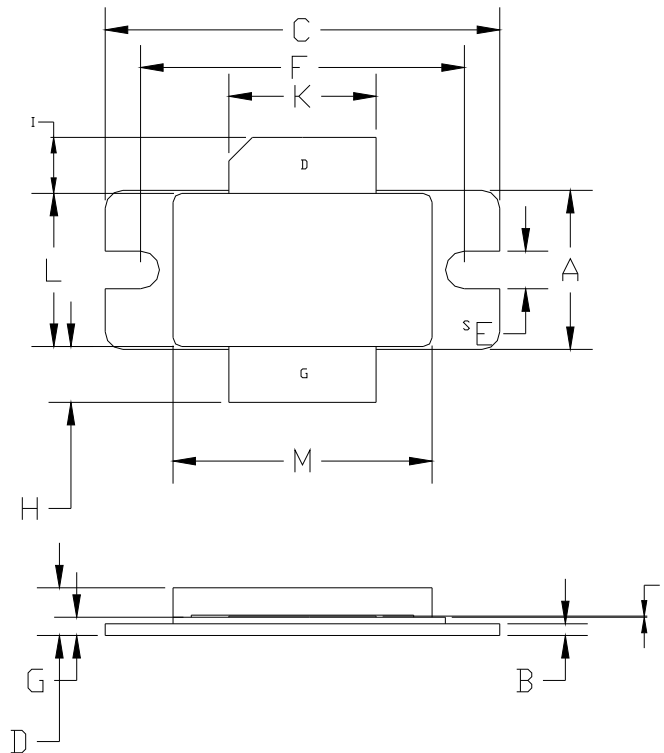
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-20	-12	-9	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Power Gain	Gp	17.45	18.00	19.45	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Efficiency	N_D	60	66	75	%	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	D	-0.50	-0.10	0.30	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power	Po	500	568	793	W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	2:1 Load Mismatch Stability	VSWR-S	2:1	--	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3,$ Rotate 2:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
100%	3:1 Load Mismatch Tolerance	LMT	3:1	--	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3,$ Rotate 3:1 output VSWR through 360° phase. Post test $P_O =$ Pre test $P_O \pm 5W$
Note 1	$V1 = 50V; I_{DQ1} = 250mA; PW1 = 444x(7\mu s \text{ ON}, 6\mu s \text{ OFF}); DF1 = 22.7\%, P_{IN1} = 9W.$						
Note 2	Test Frequencies: F1 = 960MHz, F2 = 1090MHz, F3 = 1215MHz.						
Note 3	$T_{F1} = 30 \pm 5^\circ C =$ Device flange temperature.						
Note 4	Screen 'BD' = parameter qualified By Design.						

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (MHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
960	TBD	TBD
1090	TBD	TBD
1215	TBD	TBD
Impedance Definition		

PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.535	0.545	13.58	13.84
B	0.035	0.045	0.89	1.14
C	1.335	1.345	33.90	34.16
D	0.147	0.177	3.73	4.50
E	0.123	0.133	3.12	3.37
F	1.095	1.105	27.81	28.06
G	0.057	0.067	--	--
H	0.170	0.210	4.32	5.33
I	0.170	0.210	4.32	5.33
J	0.003	0.006	0.08	0.15
K	0.495	0.505	12.57	12.82
L	0.514	0.524	13.05	13.31
M	0.871	0.889	22.12	22.58

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

RF TEST FIXTURE

TBD

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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