Part Number: IGN2325CW140 (Preliminary)

Integra
TECHNOLOGIES, INC.

S-Band General Purpose Transistor

IGN2325CW140 is an internally pre-matched, gallium nitride (GaN) high electron mobility transistor (HEMT). This part is designed for S-Band General Purpose applications operating over the 2.3 – 2.5 GHz instantaneous frequency band. Under CW conditions it supplies a minimum of 140 watts of average output power with 16dB gain typically. Specified operation is with Class AB bias. When appropriately rated it is also operable under pulsed conditions. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening.

PRELIMINARY RF DATA PRELIMINARY RF DATA PRELIMINARY RF DATA

Lot/SN:	F (GHz)	RL (dB)	Po (W)	Nd (%)	G (dB)	VSWR 3:1
50027827-2	2.30	17	140	56.9	17.8	P
	2.35	19	140	59.1	17.9	P
	2.40	18	140	60.6	17.9	P
	2.45	19	140	60.9	17.9	P
	2.50	14	140	61.9	17.2	P

Vd=32V, Idq=240mA, CW

GaN on Silicon Carbide FET
- High Power Gain
- Excellent thermal stability
- Gold Metal

Depletion Mode Device
- Negative Gate Voltage to Bias
- Bias Sequencing Required
- See App Note to Prevent Damage

Gold Metal System
- Complete Gold System
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

Class AB Operation
- Specified with AB bias

Internal Impedance Matching
- Ease of Use
- Ultra Low Loss Design

BeO Free Package
- Metal Based
- Epoxy Seal

High Power RF Test / Fixture
- Broadband
- Matched to 50 Ω (ohms)
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

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MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Breakdown Voltage	V_{DS-BK}	120	--	V	--
BD	Drain-Source Voltage	V_{DS}	--	60	V	--
BD	Gate-Source Voltage	V_{GS}	-10	0	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.5	°C/W	V_{DD}=V1, I_{DQ}=I_{DQ1}, CW, DF=DF1, T_F=25°C, P_{OUT}=140W
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Drain Leakage Current	I_{D-OFF}	--	24	--	mA	V_{DS} = 32V, V_{GS} = -8V, T_F = 25±5°C
100%	Gate Threshold Voltage	V_{GS-OFF}	--	-2.5	--	V	V_{DS} = 32V, I_D=240mA, T_F = 25±5°C

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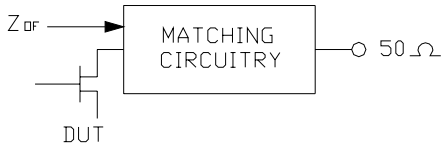
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Input Return Loss	IRL	--	-12	-9	dB	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ CW, T_F=$T_{F1,}$ P_{OUT}=P_{OUT1}, F=F1, F2, F3.
100%	Power Gain	Gp	16	17	--	dB	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ CW, T_F=$T_{F1,}$ P_{OUT}=P_{OUT1}, F=F1, F2, F3.
100%	Drain Efficiency	N_D	52	57	--	%	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ CW, T_F=$T_{F1,}$ P_{OUT}=P_{OUT1}, F=F1, F2, F3.
100%	Input Power	P_{IN}	--	2.8	3.5	W	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ CW, T_F=$T_{F1,}$ P_{OUT}=P_{OUT1}, F=F1, F2, F3.
100%	2:1 Load Mismatch Stability	VSWR-S	2:1	--	--	--	V_{DD}=V1, I_{DQ}=$I_{DQ1,}$ CW, T_F=$T_{F1,}$ P_{OUT}=P_{OUT1}, F=F1, F2, F3, Rotate output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least –65 dBc.
Note 1	V1 = 32V; I_{DQ1} = 240mA, CW, P_{OUT1} = 140W.						
Note 2	Test Frequencies: F1 = 2.3GHz, F2 = 2.4GHz, F3 = 2.5GHz.						
Note 3	T_{F1} = 25±5°C = Device flange temperature.						
Note 4	Screen 'BD' = parameter qualified By Design.						

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
2.30	2.40-j3.85	6.40-j3.60
2.35	2.35-j3.55	6.35-j3.20
2.40	2.30-j3.30	6.30-j2.90
2.45	2.30-j3.00	6.30-j2.50
2.50	2.15-j2.70	6.30-j2.10
Impedance Definition		

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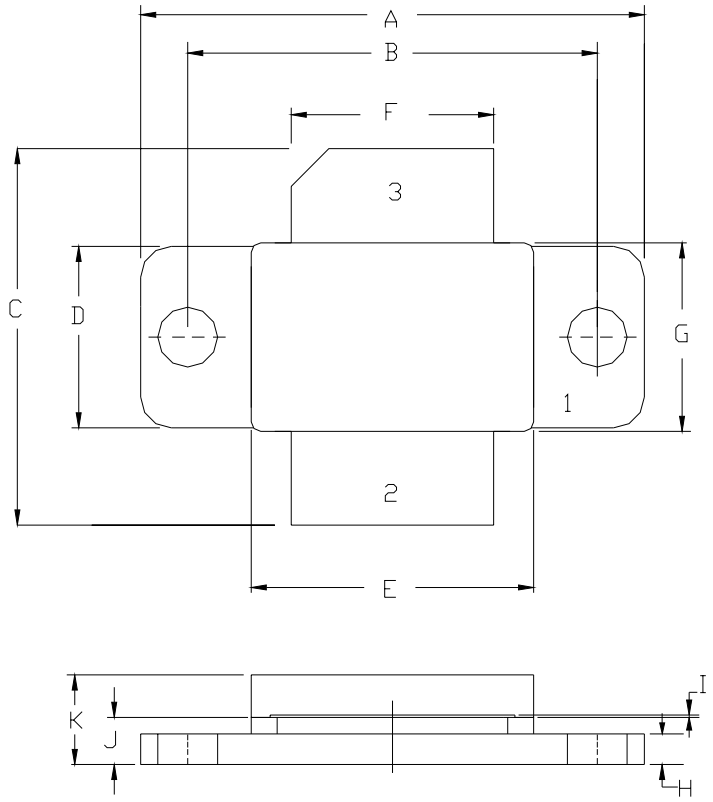
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.065	1.075	27.05	27.30
B	0.865	0.875	21.97	22.22
C	0.794	0.804	20.17	20.42
D	0.380	0.390	9.65	9.90
E	0.595	0.605	15.11	15.37
F	0.425	0.435	10.79	11.05
G	0.395	0.405	10.03	10.29
H	0.060	0.070	1.52	1.78
I	0.004	0.006	0.10	0.15
J	0.096	0.106	2.44	2.69
K	0.184	0.196	4.67	4.98

PIN SCHEDULE	
1	BASE
2	EMITTER
3	COLLECTOR

LID-P64-1

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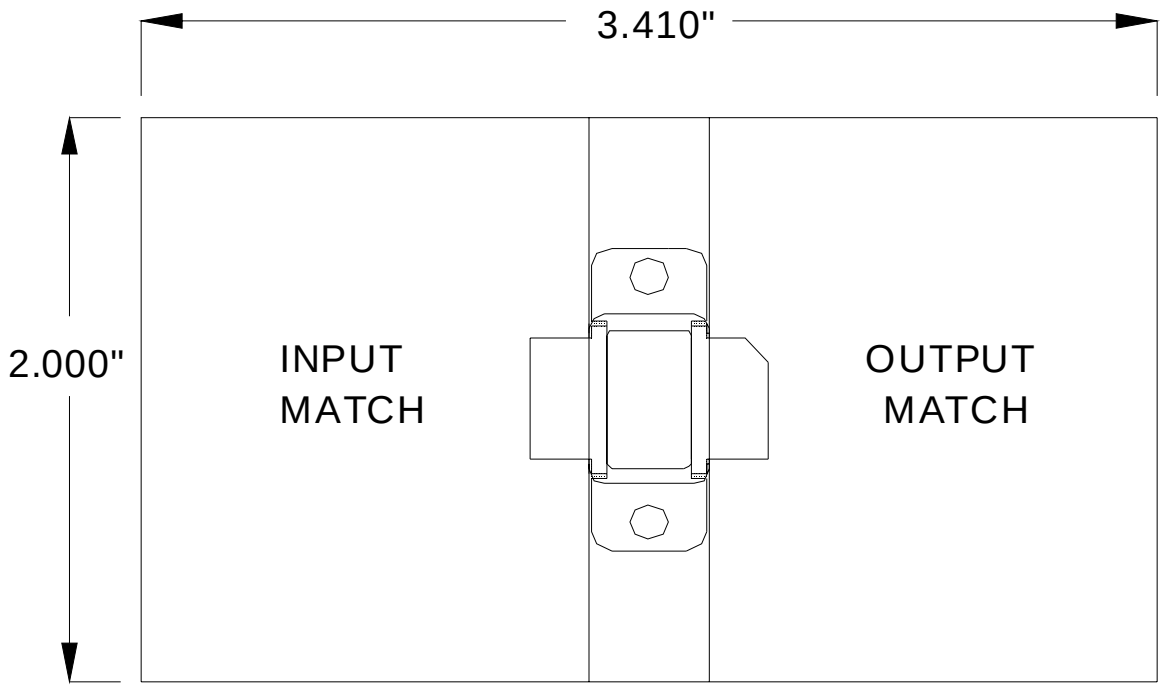
RF TEST FIXTURE



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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