

S-Band Radar Transistor

Available in a bolt down flanged version as IGN2729M500 or in a solder mount earless version IGN2729M500S. IGN2729M500 is an internally pre-matched, gallium nitride (GaN) high electron mobility transistor (HEMT). This part is designed for S-Band radar applications operating over the 2.7 – 2.9 GHz instantaneous frequency band. Under 300us / 10% pulse conditions it supplies a minimum of 500 watts of peak output power with 12dB gain typically. Specified operation is with Class AB bias. When appropriately rated, it is operable under a wide range of pulse widths and duty factors. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. This device is rated for a peak output power level of $P_{PEAK} = 500W$ @ 10% duty factor. This corresponds to an average power $P_{AVG} = 50W$.



GaN on Silicon Carbide FET

- High Power Gain
- Excellent thermal stability
- Gold Metal

Depletion Mode Device

- Negative Gate Voltage to Bias
- Bias Sequencing Required
- See App Note to Prevent Damage

Gold Metal System

- Complete Gold System
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

Class AB Operation

- Specified with AB bias

Internal Impedance Matching

- Ease of Use
- Ultra Low Loss Design

BeO Free Package

- Metal Based
- Epoxy Seal

High Power RF Test / Fixture

- Broadband
- Matched to 50 Ω (ohms)
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

SAMPLE RF DATA IN BROADBAND RF TEST FIXTURE

Lot/SN:	F	Pi	Id	RL	Po	Nd	G	D	VSWR	
	(GHz)	(W)	(A)	(dB)	(W)	(%)	(dB)	(dB)	2:1	3:1
	2.7	36	18.6	13	574	61.7	12.03	-0.12	S	P
50027112-1	2.8	36	19.73	13	625	63.4	12.40	-0.14	S	P
	2.9	36	19.64	18	615	62.6	12.33	-0.17	S	P

Vd=50V, Idq=100mA, Vgs=-2.65V, Pulse= 300 μ s-10%

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	60	V	--
BD	Gate-Source Voltage	V_{GS}	-10	0	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
BD	CW Operation	--	--	--	--	Not rated for CW operation.
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.15	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25^{\circ}C, P_{OUT}=500W$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					



DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Drain Leakage Current	I_{D-OFF}	--	--	4.0	mA	$V_{DS} = 50V, V_{GS} = -6V, T_F = 25 \pm 5^{\circ}C$
BD	Gate Threshold Voltage	V_{GS-TH}	--	-2.8	--	V	$V_{DS} = 50V, I_D = 100mA, T_F = 25 \pm 5^{\circ}C$

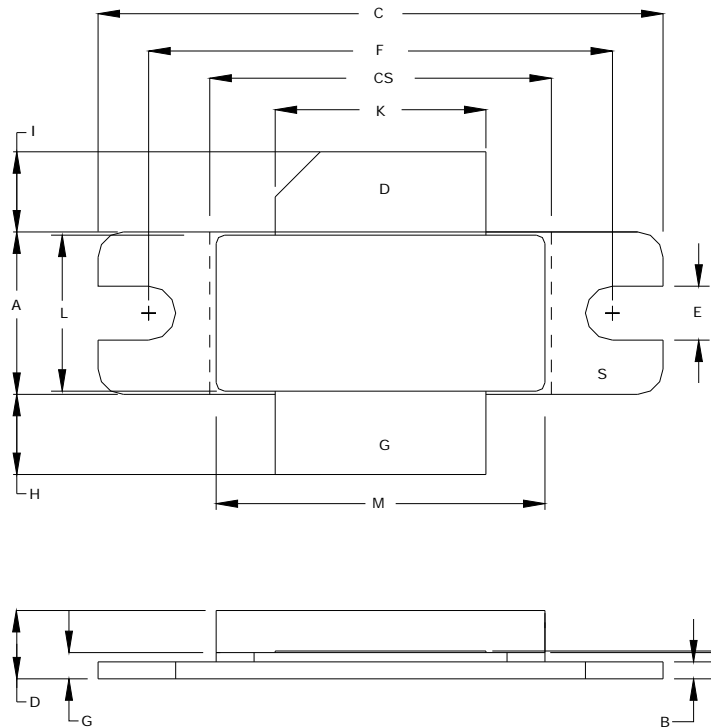
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-12	-10	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power	P_O	500	570	793	W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Power Gain	G_P	11.43	12.00	13.43	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power Flatness $10 \cdot \text{LOG}(P_{O-MAX}/P_{O-MIN})$	OPF	0	1.0	1.5	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Efficiency	N_D	55	60	75	%	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Current	I_D	13	20	29	A	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	D	-0.50	-0.25	0.30	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Insertion Phase	IP	-30	0	+30	Deg	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F3.$
100%	2:1 Load Mismatch Stability	VSWR-S	2:1	--	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$ Rotate 2:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
100%	3:1 Load Mismatch Tolerance	LMT	3:1	--	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$ Rotate 3:1 output VSWR through 360° phase. Post test $P_O = \text{Pre test } P_{O \pm 5W}$
Note 1	$V1 = 50V; I_{DQ1} = 100mA; PW1 = 300us; DF1 = 10\%, P_{IN1} = 36W.$						
Note 2	Test Frequencies: $F1 = 2.7GHz, F2 = 2.8GHz, F3 = 2.9GHz.$						
Note 3	All devices are marked with delta insertion phase dash numbers, following the part number, from -1 thru -12 indicating 5° variations between -30° to +30° from reference.						
Note 4	$T_{F1} = 25 \pm 5^\circ C = \text{Device flange temperature.}$						
Note 5	Screen 'BD' = parameter qualified By Design.						

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
2.70	2.47 -j1.76	2.47 -j2.03
2.80	2.49 -j1.69	2.35 -j1.82
2.90	2.42 -j1.76	2.49 -j1.66
Impedance Definition		

PACKAGE DIMENSIONAL OUTLINE DRAWING

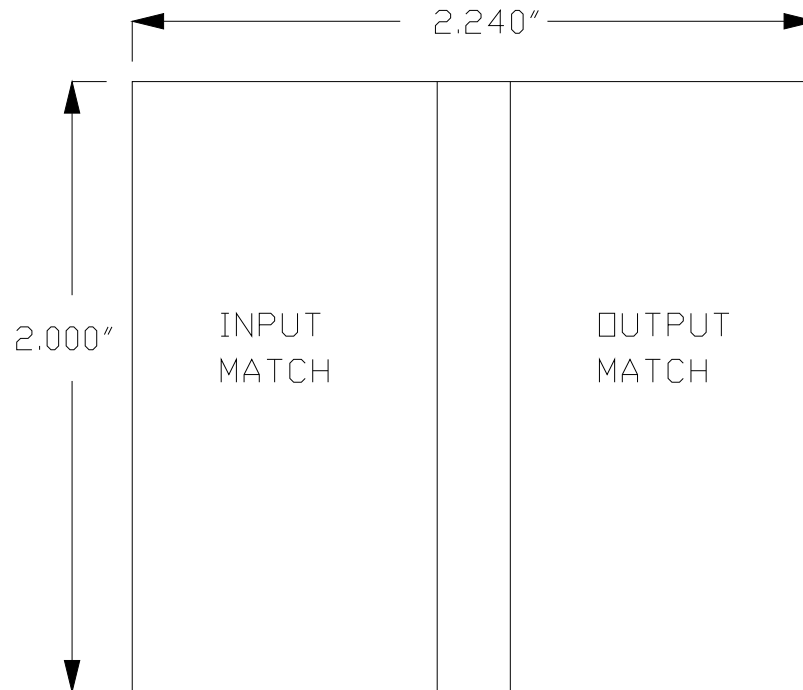


'S' VERSION USE DIM CS
NON 'S' VERSION USE DIM C

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.380	0.390	9.65	9.90
B	0.035	0.045	0.89	1.14
C	1.335	1.345	33.90	34.16
CS	0.805	0.815	20.44	20.70
D	0.139	0.166	3.53	4.21
E	0.123	0.133	3.12	3.37
F	1.095	1.105	27.81	28.06
G	0.057	0.067	1.44	1.70
H	0.170	0.210	4.32	5.33
I	0.170	0.210	4.32	5.33
J	0.003	0.006	0.08	0.15
K	0.495	0.505	12.57	12.82
L	0.364	0.374	9.24	9.49
M	0.772	0.788	19.60	20.01

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

RF TEST FIXTURE



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS AND COMPONENT LIST

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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