

# Part Number: **IGN3135M130**

# Integra

TECHNOLOGIES, INC.

## S-Band Radar Transistor

IGN3135M130 is an internally pre-matched, gallium nitride (GaN) high electron mobility transistor (HEMT). This part is designed for S-Band radar applications operating over the 3.1 – 3.5 GHz instantaneous frequency band. Under 300us / 20% pulse conditions it supplies a minimum of 130 watts of peak output power with 12dB gain typically. Specified operation is with Class AB bias. When appropriately rated, it is operable under a wide range of pulse widths and duty factors. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. This device is rated for a peak output power level of  $P_{PEAK} = 130W$  @ 20% duty factor. This corresponds to an average power  $P_{AVG} = 26W$ .



### SAMPLE RF DATA IN BROADBAND RF TEST FIXTURE

| Lot/SN:    | F (GHz) | Pi (W) | Id (A) | RL (dB) | Po (W) | Nd (%) | G (dB) | Drp (dB) | VSWR |     |
|------------|---------|--------|--------|---------|--------|--------|--------|----------|------|-----|
|            |         |        |        |         |        |        |        |          | 2:1  | 3:1 |
| 50025866-2 | 3.1     | 10     | 8.135  | -18     | 143    | 54.9   | 11.55  | -0.15    | S    | P   |
|            | 3.3     | 10     | 8.165  | -18     | 148    | 56.6   | 11.70  | -0.06    | S    | P   |
|            | 3.5     | 10     | 6.815  | -18     | 140    | 64.2   | 11.46  | -0.09    | S    | P   |

Vd=32V, Idq=30mA, Pulse 300us/20%

### GaN on Silicon Carbide FET

- High Power Gain
- Excellent thermal stability

### Depletion Mode Device

- Negative Gate Voltage to Bias
- Bias Sequencing Required
- See App Note to Prevent Damage

### Gold Metal System

- Complete Gold System
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

### Class AB Operation

- Specified with AB bias

### Internal Impedance Matching

- Ease of Use
- Ultra Low Loss Design

### BeO Free Package

- Metal Based
- Epoxy Seal

### High Power 50Ω RF Test / Fixture

- Broadband
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

### Patent Issued

- US 8,299,857 B2

**MAXIMUM RATINGS**

| Screen | Parameter                                    | Symbol    | Min | Max  | Units | Test Conditions            |
|--------|--|-----------|-----|------|-------|----------------------------|
| BD     | Drain-Source Voltage                         | $V_{DS}$  | --  | 40   | V     | --                         |
| BD     | Gate-Source Voltage                          | $V_{GS}$  | -10 | 0    | V     | --                         |
| BD     | Storage Temperature Range                    | $T_{STG}$ | -55 | +150 | °C    | --                         |
| BD     | Operating Junction Temperature Range         | $T_J$     | -55 | +200 | °C    | --                         |
| BD     | CW Operation                                 | --        | --  | --   | --    | Not rated for CW operation |
| Note   | Screen 'BD' = parameter qualified By Design. |           |     |      |       |                            |

**THERMAL CHARACTERISTICS**

| Screen | Parameter                                    | Symbol       | Min | Max  | Units | Test Conditions   |
|--------|--|--------------|-----|------|-------|---|
| BD     | Thermal Resistance                           | $R_{TH(JC)}$ | --  | 0.50 | °C/W  | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=130W$ |
| Note   | Screen 'BD' = parameter qualified By Design. |              |     |      |       |   |

**PROCESSING SPECIFICATIONS**

| Screen | Parameter  | Symbol | Min | Max | Units | Test Conditions                               |
|--------|--|--------|-----|-----|-------|---|
| 100%   | DC Wafer Probe   | --     | --  | --  | --    | Per Integra specification.                    |
| Q1     | Wafer DC and RF Qualification  | --     | --  | --  | --    | Per Integra specification.                    |
| LM     | Wire Bond Strength   | --     | --  | --  | --    | Line monitor per Integra specification.       |
| 100%   | Pre-cap visual inspection  | --     | --  | --  | --    | Per Integra specification                     |
| 100%   | Gross leak test  | --     | --  | --  | --    | MIL-STD-750D, Method 1071.6, Test Condition C |
| Note   | Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer. |        |     |     |       |   |
| Note   | Screen 'LM' = parameter is qualified by assembly line monitor.                           |        |     |     |       |   |

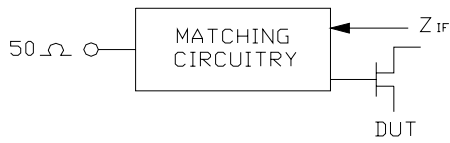

**DC ELECTRICAL CHARACTERISTICS**

| Screen | Parameter              | Symbol      | Min | Typ  | Max | Units | Test Conditions                                      |
|--------|------------------------|-------------|-----|------|-----|-------|--|
| BD     | Drain Leakage Current  | $I_{D-OFF}$ | --  | 0.4  | 8.0 | mA    | $V_{DS} = 32V, V_{GS} = -8V, T_F = 25 \pm 5^\circ C$ |
| BD     | Gate Threshold Voltage | $V_{GS-TH}$ | --  | -3.5 | --  | V     | $V_{DS} = 32V, I_D = 100mA, T_F = 25 \pm 5^\circ C$  |

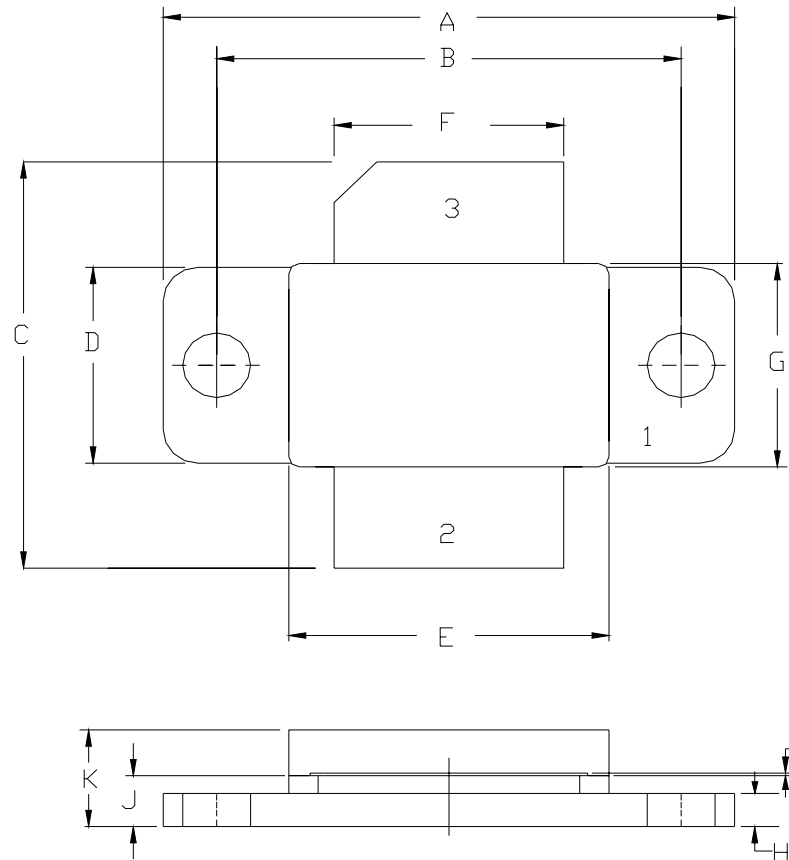
**RF ELECTRICAL CHARACTERISTICS**

| Screen | Parameter  | Symbol   | Min   | Typ   | Max   | Units | Test Conditions   |
|--------|--|----------|-------|-------|-------|-------|---|
| 100%   | Input Return Loss  | IRL      | -20   | -12   | -10   | dB    | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | Power Gain   | Gp       | 11.14 | 12.20 | 13.14 | dB    | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | Drain Efficiency   | $\eta_D$ | 50    | 66    | 80    | %     | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | Pulse Amplitude Droop  | D        | -0.50 | 0     | 0.30  | dB    | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | Output Power   | Po       | 130   | 166   | 206   | W     | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | 2:1 Load Mismatch Stability  | VSWR-S   | 2:1   |       | --    | --    | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3,$ Rotate 2:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc. |
| 100%   | 3:1 Load Mismatch Tolerance  | LMT      | 3:1   | TBD   | --    | --    | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3,$ Rotate 3:1 output VSWR through 360° phase. Post test $P_O =$ Pre test $P_O \pm 5W$   |
| Note 1 | $V1 = 32V; I_{DQ1} = 30mA; PW1 = 300us; DF1 = 20%, P_{IN1} = 10W.$ |          |       |       |       |       |   |
| Note 2 | Test Frequencies: F1 = 3.1GHz, F2 = 3.3GHz, F3 = 3.5GHz.           |          |       |       |       |       |   |
| Note 3 | $T_{F1} = 25 \pm 5^\circ C =$ Device flange temperature.           |          |       |       |       |       |   |
| Note 4 | Screen 'BD' = parameter qualified By Design.                       |          |       |       |       |       |   |

**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

| Frequency (GHz)      | $Z_{IF} (\Omega)$  | $Z_{OF} (\Omega)$   |
|----------------------|--|---|
| 3.1                  | 8.7 -j6.4  | 9.1 -j2.2   |
| 3.3                  | 7.8 -j5.9  | 8.8 -j2.5   |
| 3.5                  | 8.3 -j3.9  | 8.6 -j1.1   |
| Impedance Definition |  |  |

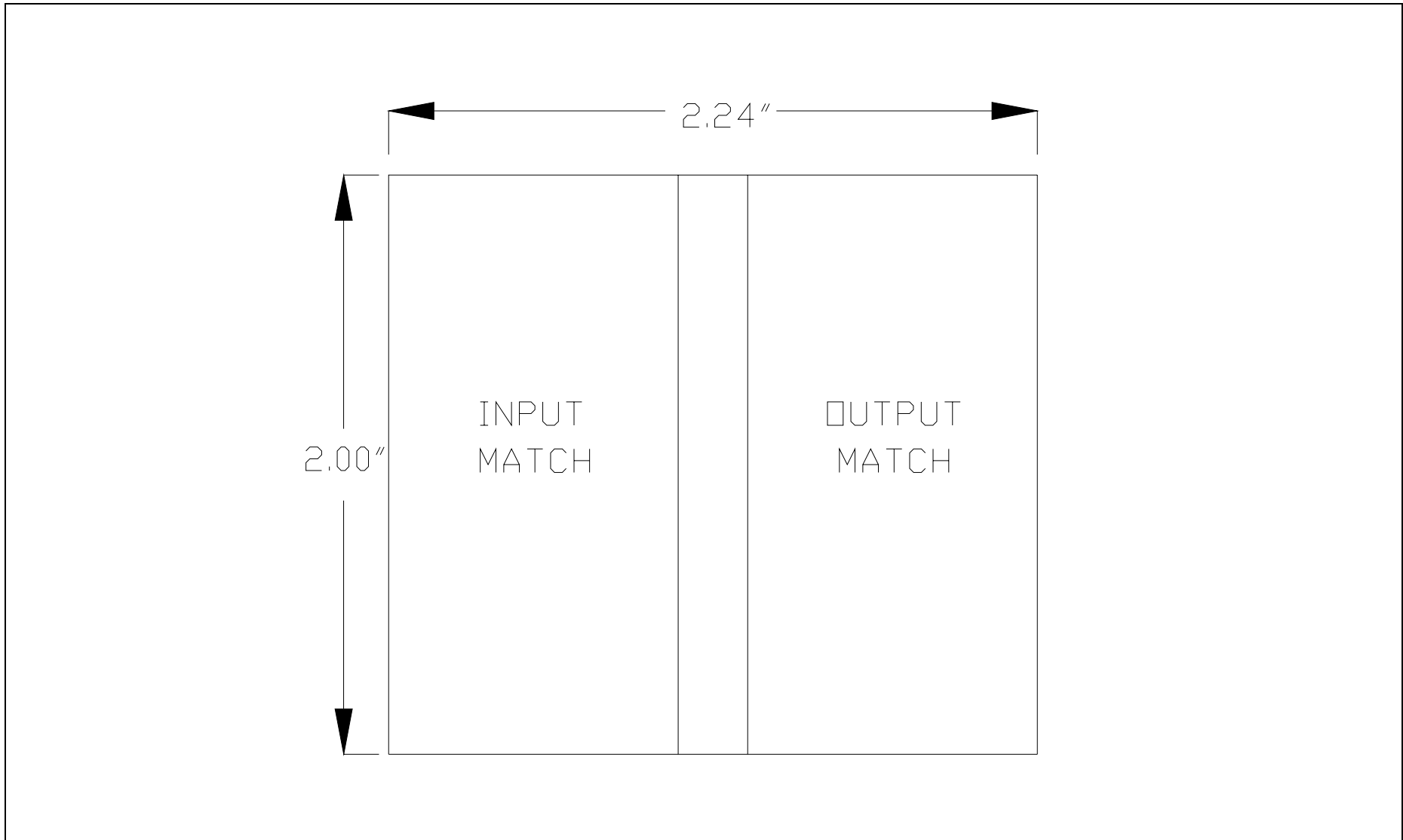
**PACKAGE DIMENSIONAL OUTLINE DRAWING**



| DIM | INCHES |       | MILLIMETERS |       |
|-----|--------|-------|-------------|-------|
|     | MIN    | MAX   | MIN         | MAX   |
| A   | 1.065  | 1.075 | 27.05       | 27.30 |
| B   | 0.865  | 0.875 | 21.97       | 22.22 |
| C   | 0.794  | 0.804 | 20.17       | 20.42 |
| D   | 0.380  | 0.390 | 9.65        | 9.90  |
| E   | 0.595  | 0.605 | 15.11       | 15.37 |
| F   | 0.425  | 0.435 | 10.79       | 11.05 |
| G   | 0.395  | 0.405 | 10.03       | 10.29 |
| H   | 0.060  | 0.070 | 1.52        | 1.78  |
| I   | 0.004  | 0.006 | 0.10        | 0.15  |
| J   | 0.096  | 0.106 | 2.44        | 2.69  |
| K   | 0.184  | 0.196 | 4.67        | 4.98  |

| PIN SCHEDULE |           |
|--------------|-----------|
| 1            | BASE      |
| 2            | EMITTER   |
| 3            | COLLECTOR |

**RF TEST FIXTURE**



**CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS**

**DEFINITIONS**

| <b>Data Sheet Status</b>   |   |
|--|---|
| Proposed Specification   | This data sheet contains proposed specifications.                                   |
| Preliminary Specification  | This data sheet contains specifications based on preliminary measurements and data. |
| Product Specification  | This data sheet contains final product specifications.                              |
| <b>Maximum Ratings</b>   |   |
| Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability. |   |

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