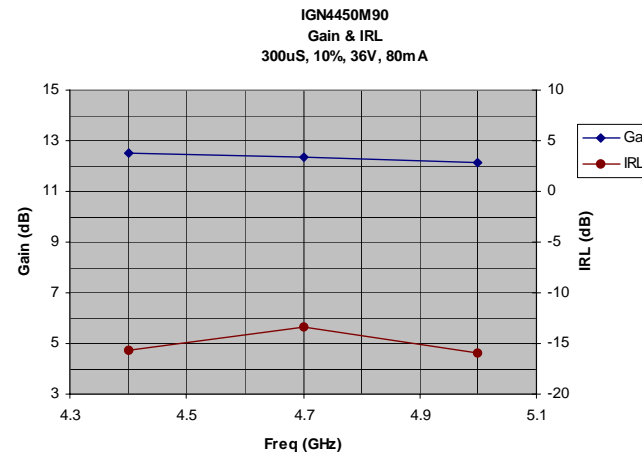
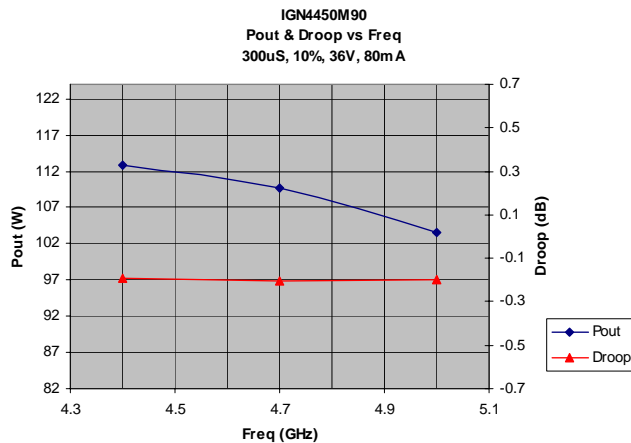


## C-Band Radar Transistor

IGN4450M90 is an internally pre-matched, gallium nitride (GaN) high electron mobility transistor (HEMT). This part is designed for C-Band radar applications operating over the 4.4 – 5.0 GHz instantaneous frequency band. Under 300us / 10% pulse conditions it supplies a minimum of 90 watts of peak output power with 13dB gain typically. Specified operation is with Class AB bias. When appropriately rated, it is operable under a wide range of pulse widths and duty factors. It operates with spectral purity into all phases of 3:1 output VSWR. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. This device is rated for a peak output power level of  $P_{PEAK} = 90W$  @ 10% duty factor. This corresponds to an average power  $P_{AVG} = 9.0W$ .



## TYPICAL RF DATA



### GaN on Silicon Carbide FET

- High Power Gain
- Excellent Thermal Stability
- Gold Metal

### Gold Metal System

- Complete Gold System
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

### Class AB

- Specified with AB bias

### Internal Impedance Matching

- Ease of Use
- Input and Output
- Ultra Low Loss Design

### Metal - Ceramic

- Metal Based
- Epoxy Seal

### High Power 50Ω RF Test / Fixture

- Broadband
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

### Patent Issued

- US 8,299,857 B2

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Breakdown Voltage	$V_{DS-BK}$	80	--	V	--
BD	Drain-Source Voltage	$V_{DS}$	--	40	V	--
BD	Gate-Source Voltage	$V_{GS}$	-10	0	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
BD	CW Operation	--	--	--	--	Not rated for CW operation.
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.26	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=90W, N_D=50\%$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					



**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Drain Leakage Current	$I_{D-OFF}$	--	0.4	--	mA	$V_{DS} = 36V, V_{GS} = -8V, T_F = 25\pm5^\circ C$
100%	Gate Threshold Voltage	$V_{GS-TH}$	--	-3.5	--	V	$V_{DS} = 36V, I_D = 0.500A, T_F = 25\pm5^\circ C$

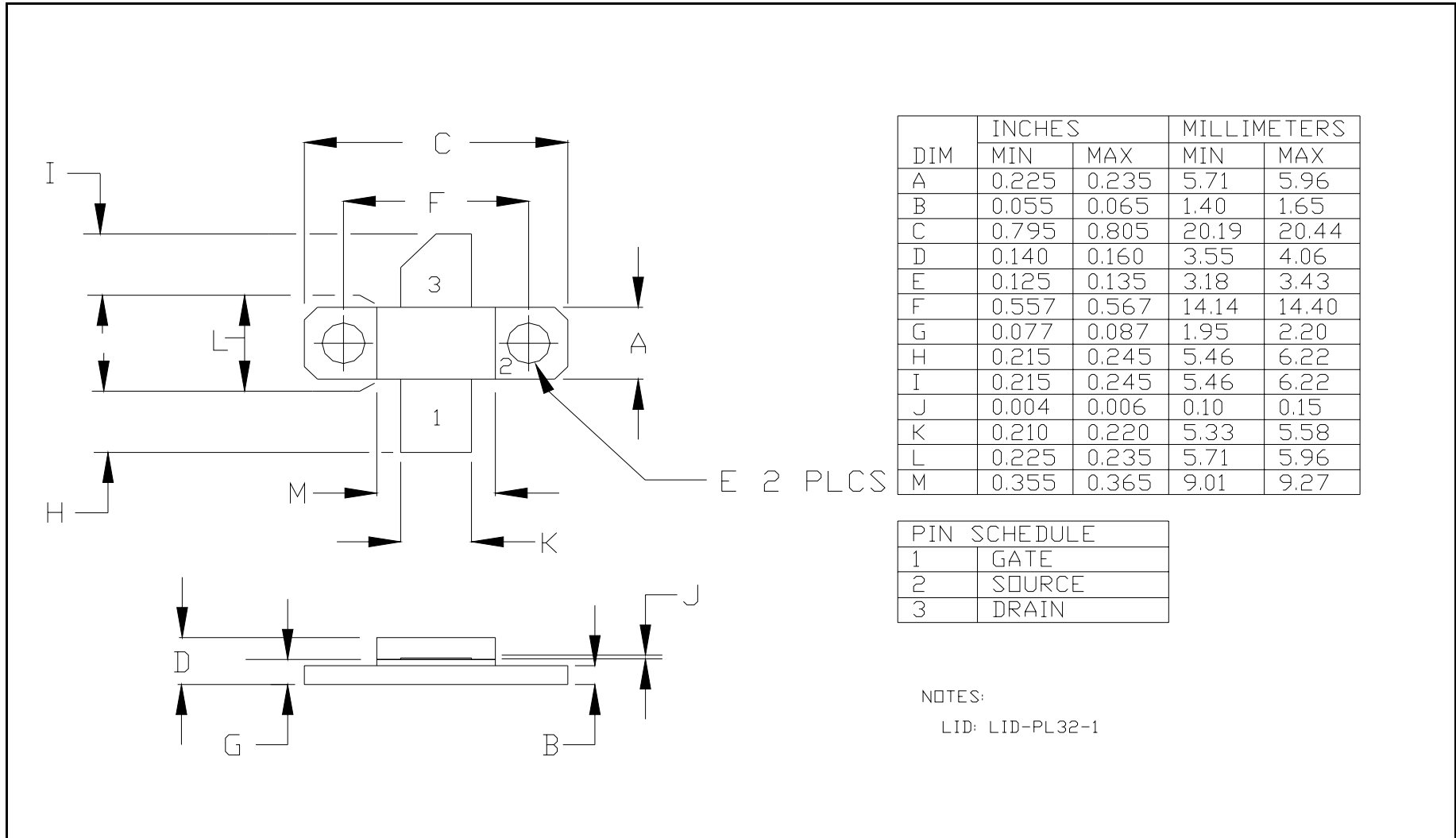
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-8	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power	$P_O$	90	143	W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Efficiency	$\eta_d$	50	75	%	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	Droop	0.5	-0.5	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Power Gain	$G_p$	12.55	14.56	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	3:1 Load Mismatch Stability	VSWR-S	S	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.$ Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
Note 1	$V1 = 36V; I_{DQ1} = 80mA; PW1 = 300\mu s; DF1 = 10\%$					
Note 2	Input Power Test Levels: $P_{IN1} = 5W$					
Note 3	Output Power Test Levels: $P_{OUT1} = 90W$					
Note 4	Test Frequencies: $F1 = 4.4 \text{ GHz}, F2 = 4.7 \text{ GHz}, F3 = 5.0 \text{ GHz}.$					
Note 5	$T_{F1} = 25 \pm 5^\circ C =$ Device flange temperature.					
Note 6	Screen 'BD' = parameter qualified By Design.					

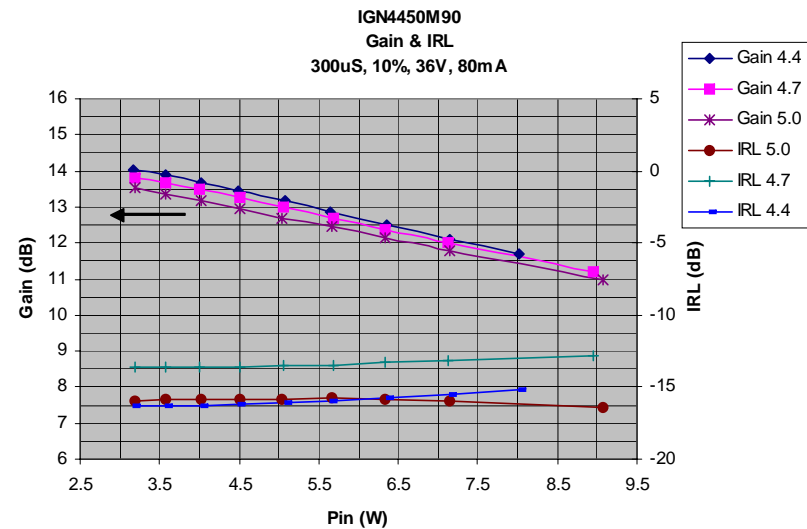
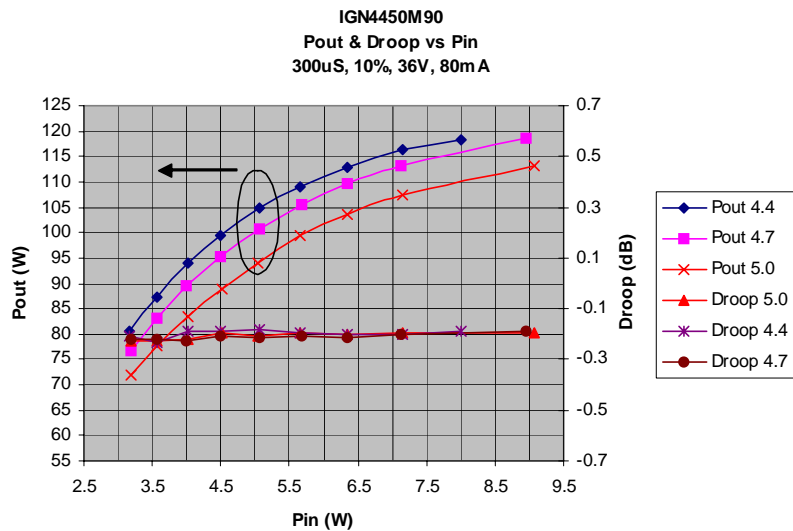
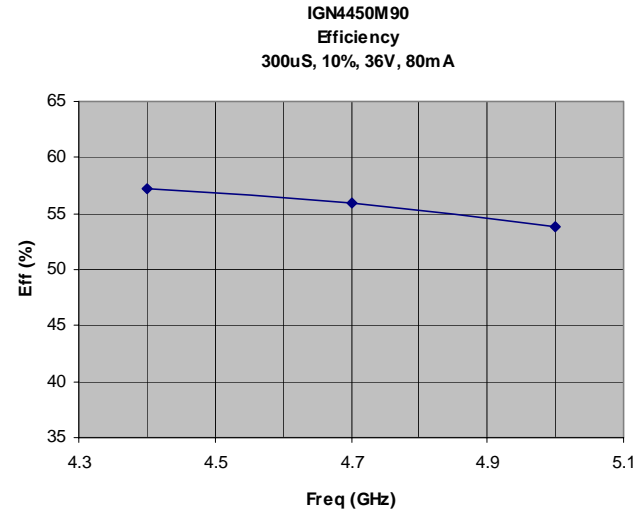
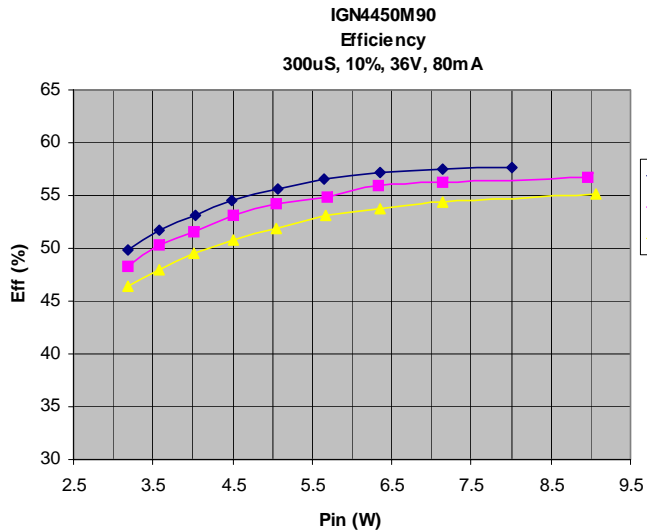
**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (GHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
4.4	$4.4 - j8.6$	$5.6 - j5.7$
4.7	$4.4 - j6.8$	$5.6 - j4.5$
5.0	$4.4 - j5.2$	$5.6 - j3.2$
Impedance Definition		

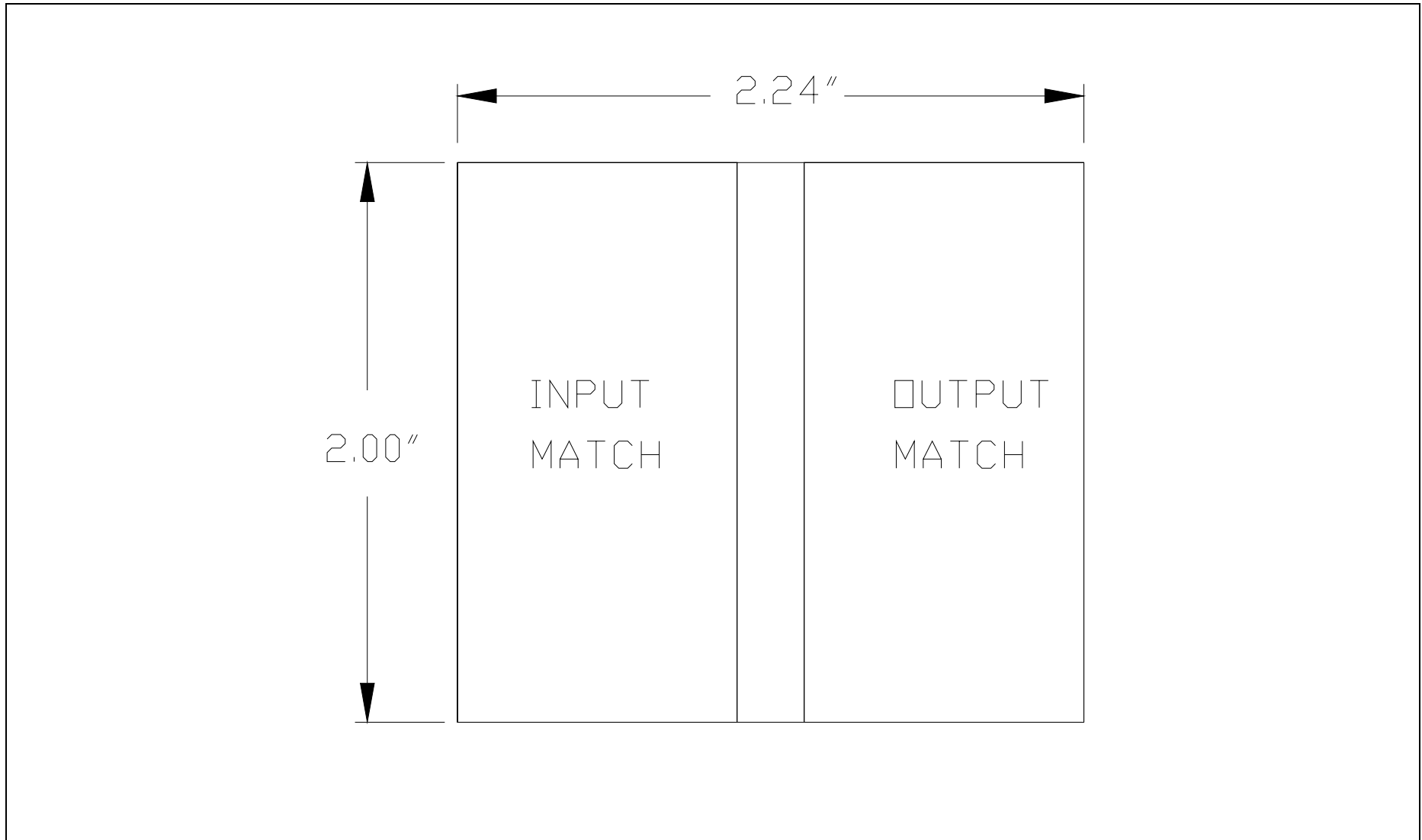
**PACKAGE DIMENSIONAL OUTLINE DRAWING**



**RF PERFORMANCE GRAPHS**



RF TEST FIXTURE



**CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS**

**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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