Part Number: ILD0506EL350

Integra
TECHNOLOGIES, INC.

P-Band RF Power LDMOS Transistor

The high power pulsed transistor part number ILD0506EL350 is designed for P-Band systems operating at 480-610 MHz. Operating at a pulse width of 15ms with a duty factor of 33%, this push-pull MOSFET device supplies a minimum of 350 watts of peak pulse power across the instantaneous operating bandwidth of 480-610 MHz. Fabricated with all gold metal contact, wire bonding and package for maximum reliability. All devices are 100% screened for large signal RF parameters in the broadband RF test fixture across the entire specified operating bandwidth with no variable or external tuning.

Silicon LDMOS
- High Power Gain
- Superior thermal stability

Class AB Operation
- Gate biased to I_{DQ}=2x100mA

Configuration
- Push-Pull

Gold Metal
- Gold Chip Metal
- Gold Wire Bond
- Maximum Reliability

Package
- Thermally Enhanced
- Gold Metal based

Epoxy Sealed Lid
- Gross Leak Qualified

RF Test Fixture
- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

Freq (GHz)	Pin (W)	IRL (dB)	Pout (W)	Gain (dB)	Nd (%)	Droop (dB)
0.480	10.5	-8	350	15.3	56.4	0
0.545	11.8	-9.5	350	14.8	53	0
0.610	12.7	-19	350	14.4	53.8	-0.1
0.480	8.6	-7.7	300	15.5	53	0
0.545	10.2	-9	300	14.7	49.3	0
0.610	10.2	-19	300	14.7	51	0

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MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	TBD	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	+12	V	--
BD	Storage Temperature Range	T_{STG}	-40	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	TBD	°C/W	V_{CC}=45V, I_{DQ}=2x100mA, T_F=70±5°C, P_{OUT}=350W
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage (each side)	BV_{DSS}	TBD	100	--	V	I_D = 10mA, V_{GS} = 0V, T_F = 25±5°C
100%	Drain Leakage Current (each side)	I_{DSS}	--	5	TBD	µA	V_{DS} = 45V, V_{GS} = 0V, T_F = 25±5°C
100%	Gate Threshold Voltage (each side)	V_{GSTH2}	TBD	3.8	TBD	V	I_D = 0.1A, V_{DS} = 45V, T_F = 25±5°C

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RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Input Return Loss	IRL	--	-7	--	dB	V_{DD}=V1; I_{DQ}=I_{DQ1}: T_F=T_{F1}: P_{out}= P_{OUT1}: F=F1 ;PW1, DF1
100%	Input Return Loss	IRL	--	-8	--	dB	V_{DD}=V1; I_{DQ}=I_{DQ1}: T_F=T_{F1}: P_{out}= P_{OUT1}: F=F2 ;PW1, DF1
100%	Input Return Loss	IRL	--	-12	--	dB	V_{DD}=V1; I_{DQ}=I_{DQ1}: T_F=T_{F1}: P_{out}= P_{OUT1}: F=F3 ;PW1, DF1
BD	Output Power- P1dB	P_O	--	350	--	W	V_{DD}=V1; I_{DQ}=I_{DQ1}: T_F=T_{F1}: F=F1, F2, F3 ; PW1, DF1
100%	Power Gain	G_P	--	14	--	dB	V_{DD}=V1; I_{DQ}=I_{DQ1}: T_F=T_{F1}: P_{out}= P_{OUT1}: F=F1, F2, F3 ;PW1, DF1
100%	Drain Efficiency	N_D	--	53		%	V_{DD}=V1; I_{DQ}=I_{DQ1}: T_F=T_{F1}: P_{out}= P_{OUT1}: F=F1, F2, F3 ;PW1, DF1
100%	Pulse Amplitude Droop	D	--	0	--	dB	V_{DD}=V1; I_{DQ}=I_{DQ1}: T_F=T_{F1}: P_{out}= P_{OUT1}: F=F1, F2, F3 ;PW1, DF1
100%	Gain Flatness versus Frequency	GF	--	1	--	dB	V_{DD}=V1; I_{DQ}=I_{DQ1}: T_F=T_{F1}: P_{out}= P_{OUT1}: F=F1, F2, F3 ;PW1, DF1
100%	Stability into 2:1 VSWR	VSWR-S	--	--	--	--	V_{DD}=V1; I_{DQ}=I_{DQ1}: T_F=T_{F1}: P_{out}= P_{OUT1}: F=F1, F2, F3 ;PW1, DF1 Rotate 2:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	3:1 Load Mismatch Tolerance	LMT	--	--	--	--	V_{DD}=V1; I_{DQ}=I_{DQ1}: T_F=T_{F1}: P_{out}= P_{OUT1}: F=F1, F2, F3 ;PW1, DF1 Rotate 3:1 output VSWR through 360° phase. Post test P_O = Pre test P_O±15W.
Note	V1=45 V; I_{DQ1}=100 mA/side; PW1=15ms; DF1=33%; T_{F1}=40±5°C; P_{OUT1}=350 W; F1=480MHz, F2=545MHz, F3=610MHz						

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (MHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
480	3.2 –j2.4	7.3 –j4.6
545	3.7 –j0.7	6.7 –j2.2
610	4.2 +j0.9	7.2 +j0.2
Impedance Definition	Test Fixture Input Impedance Measured with Push-Pull probe	Test Fixture Output Impedance Measured with Push-Pull probe

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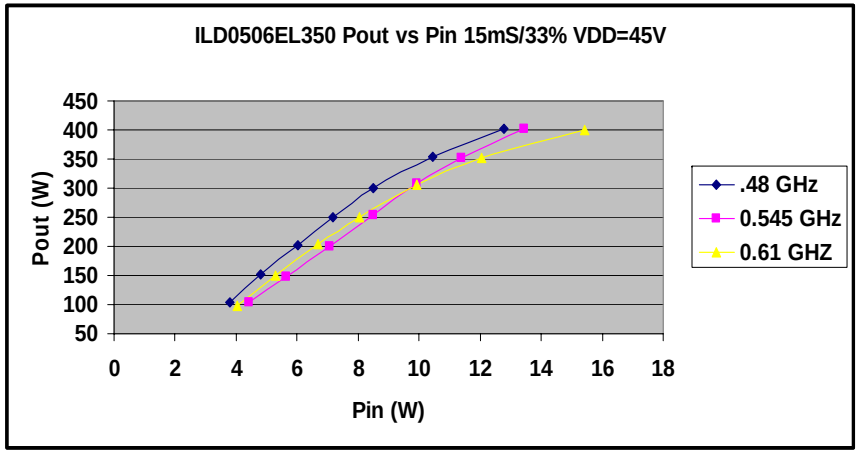
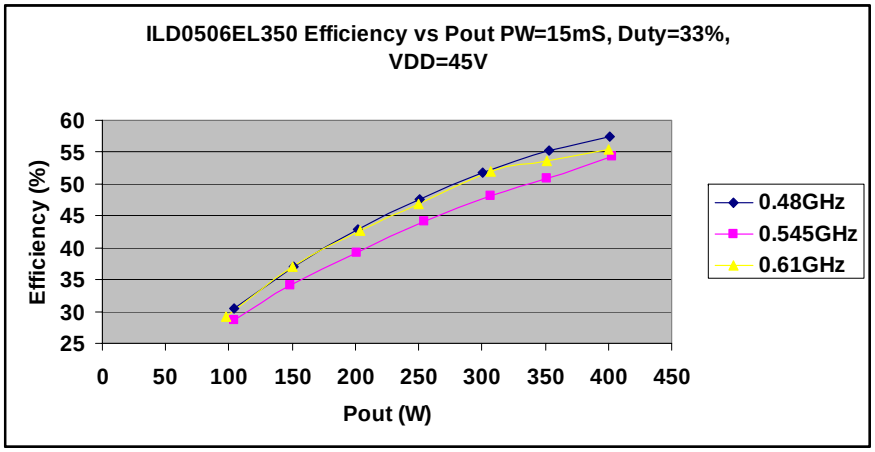
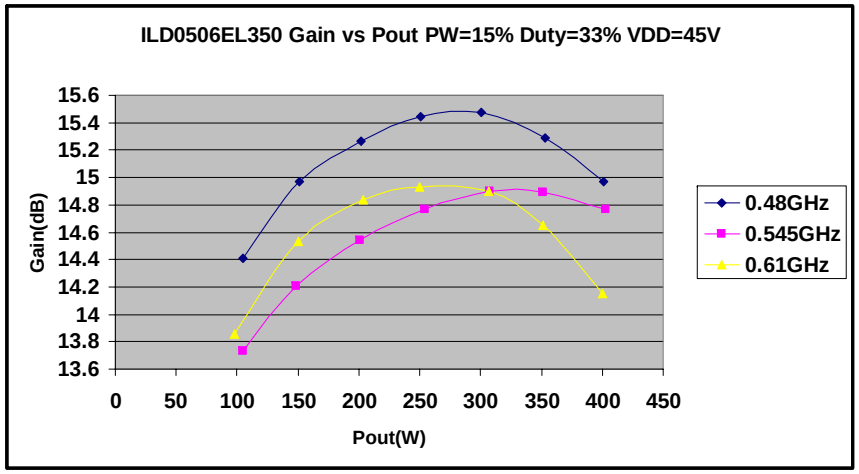
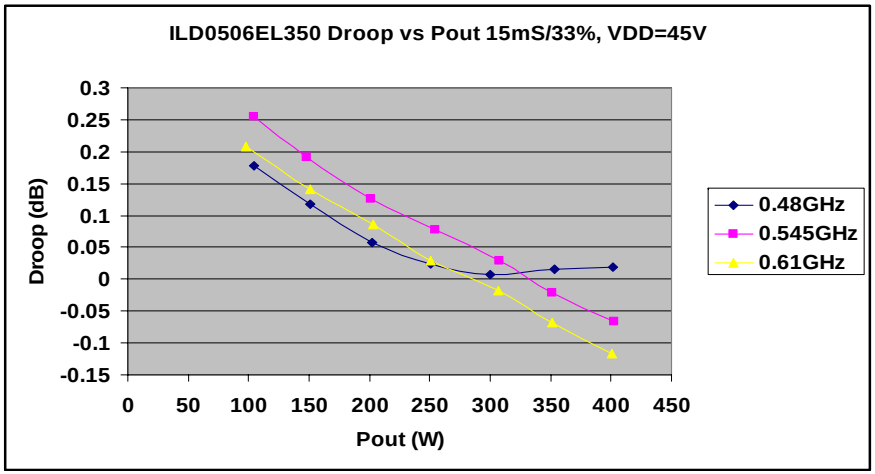
TYPICAL DEVICE RF DATA









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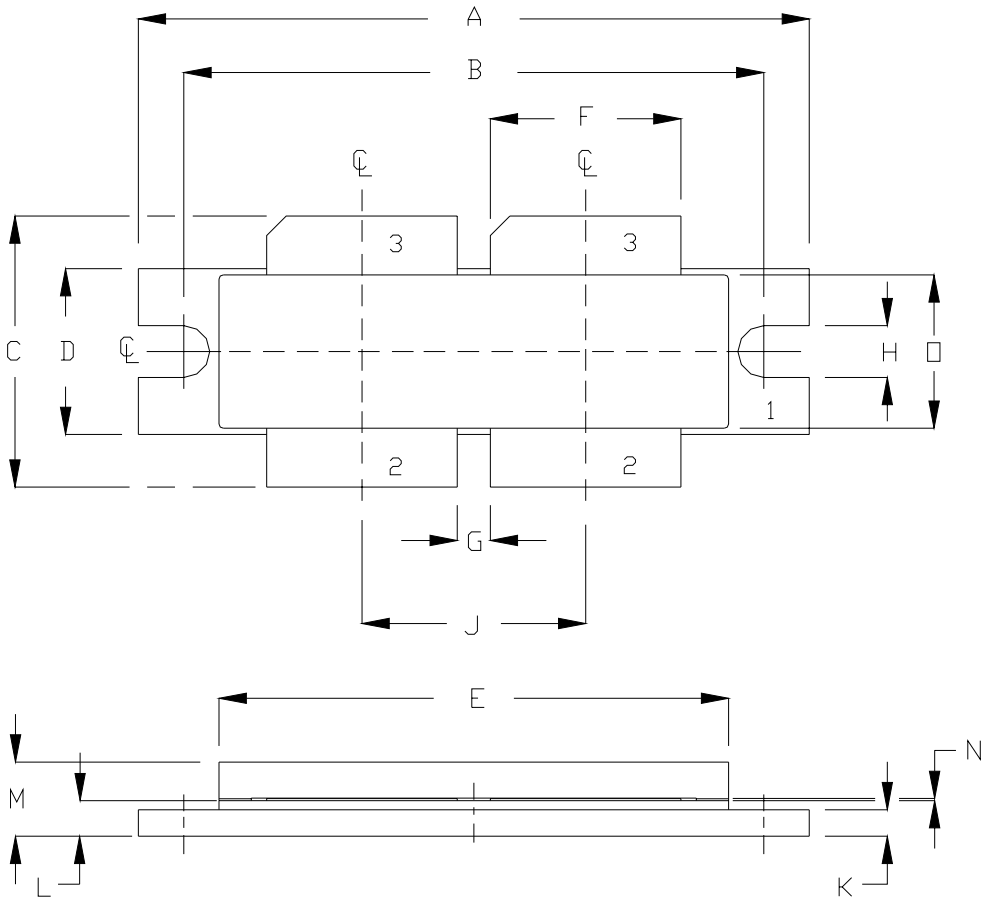
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.27
B	1.395	1.405	35.43	35.69
C	0.634	0.674	16.10	17.12
D	0.395	0.405	10.03	10.29
E	1.219	1.241	30.96	31.52
F	0.455	0.465	11.56	11.81
G	0.075	0.085	1.90	2.16
H	0.120	0.130	3.05	3.30
J	0.535	0.545	13.59	13.84
K	0.059	0.069	14.99	17.53
L	0.081	0.091	2.06	2.31
M	0.164	0.194	4.16	4.93
N	0.004	0.007	0.10	0.18
□	0.354	0.364	8.99	9.24

PIN SCHEDULE	
1	SOURCE
2	GATE
3	DRAIN

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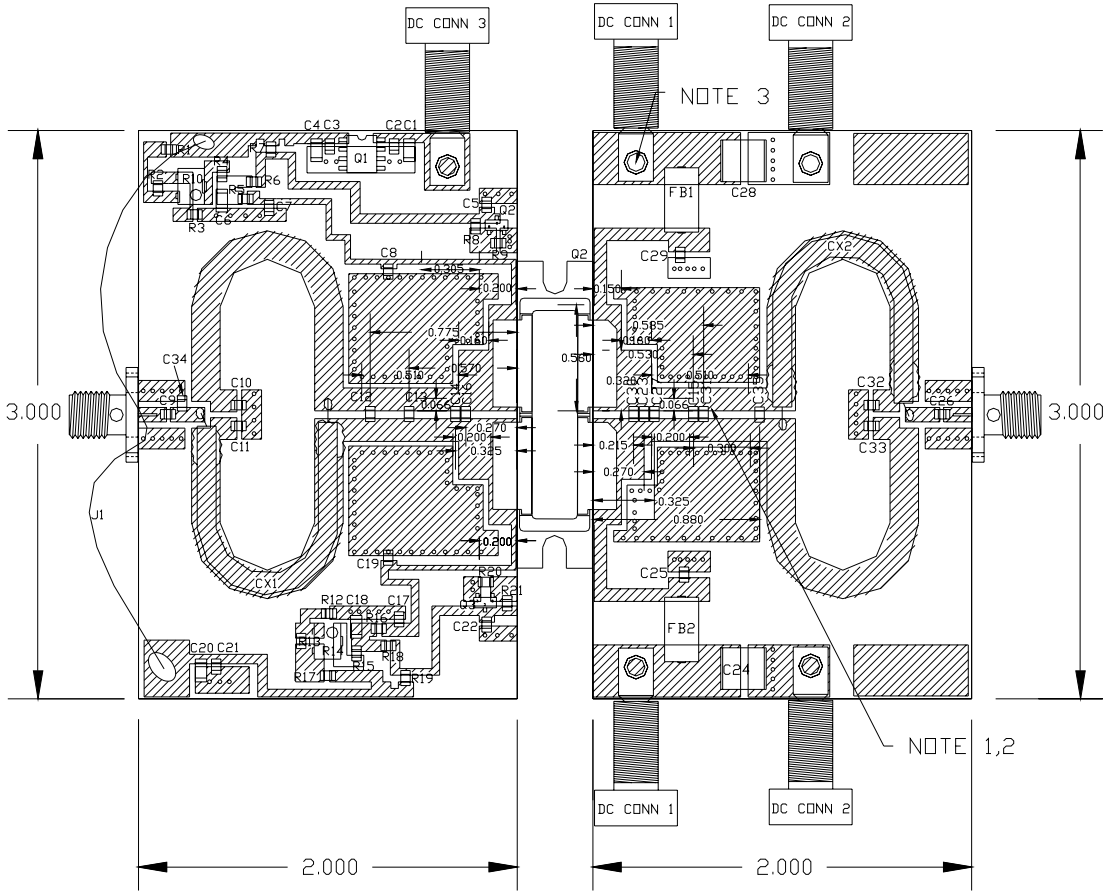
RF TEST FIXTURE ASSEMBLY



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS
L:\Public\Controlled Documents\Controlled Drawings\RF Test Fixture Drawings\ILD0506EL350 REV NC.dwg

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RF TEST FIXTURE ASSEMBLY PART LIST

COMPONENT	DESCRIPTION
DUT	TRANSISTOR #ILD403 MOUNT HARD TO THE RIGHT
PC BOARD	IPC66
C1, C4, C6, C18, C20	CAPACITOR 1uF, 1206, NURATA GRM31CR72A105KA01L
C2, C3, C5, C7, C8, C9, C10, C11, C17, C19, C21, C22, C25, C26, C29, C32, C33,	CAPCITOR 0805 100pF , ATC 600F
C12	CAPCITOR 3.3pF, 0805, +/- 0.25PF ATC 600F3R3CT250X
C13	CAPACITOR 10pF, 0805, +/- 5% ATC 600F100CT250X
C14	CAPACITOR 18pF, 0805, +/- 5% ATC 600F180CT250X
C15, C23, C27	CAPACITOR 5.6pF, 0805, +/- 0.25pF ATC 600F5R6CT250X
C16	CAPACITOR 3.9pF, 0805, +/- 5% ATC 600F3R9CT250X
C24, C28	CAPACITOR 10UF, 2220, TDK, C5750X7R1H106M
C30	CAPACITOR 6.8pF, 0805, +/- 5% ATC 600F6R8CT250X
C31	CAPACITOR 4.7pF, 0805, +/- 0.25pF ATC 600F4R7CT250X
C34	CAPACITOR 0805 AS REQUIRED FOR GAIN SLOPE
C35	CAPACITOR 39pF, 0805, +/-0.25pF ATC 600F3R0CT250X
FB1, FB2	IND, FERRITE, 10A, STEWARD 28F0181-1SR-10
Q1	IC, REG, 8V, LN78L08
Q2, Q3	TRAN, NPN, 2N2222 MARKES (1P 1)
R1, R2, R13, R17	RESISTOR 180, 0805 (180)
R3, R12	RESISTOR 150, 0805 (151)
R4, R15	RESISTOR 470, 0805 (470)

COMPONENT	DESCRIPTION
R5, R16	RESISTOR 5R1, 0805 (5.1)
R6, R18	RESISTOR 1.5K, 0805 (152)
R7, R9, R19, R20	RESISTOR 1K, 0805 (102)
R8, R21	RESISTOR 8.2K, 0805 (822)
R10, R14	RESISTOR, POT, 200 #3224W-1-201E
CX1, CX2	COAX, 25OHM, 2.3", 0.085 DIA, MICRO-COAX, UT-85C-25 (SOLDER AT 4 PLACES AS SHOWN)
J1	JUMPER WIRE 24 AWG. BLUE SUPPORT THROUGH SMA TOP HOLES
GS	PLATED THRU VIAS COPPER TH=0.001
CONN 1, CONN 2	SMA CONNECTOR, OS #2052-5636-02
INPUT PCB CARRIER	3 INCH BRASS -01
OUTPUT PCB CARRIER	3 INCH BRASS -01
TRANSISTOR CARRIER	4 INCH CARRIER -01
TRANSISTOR CLAMP	NORYL CLAMP DUAL -01
ALUMINUM HEAT SINK	4 INCH HEAT SINK -03
DC ONN 1	BANANA JACK, RED
DC CONN 2	BANANA JACK, BLACK
DC CONN 3	BANANA JACK, BLUE
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST
	1. MOUNT ALL CHIP CAPS WIDE SIDE DOWN (NOT ON EDGE)
	2. CRITICAL TUNING CAP LOCATIONS INDICATED FROM PCB EDGE
	3. JACKS INSTALLED WITH SHOULDER WASHER (#3229) AND 2-56 SCREW (5PL). JACK =SHOULD NOT SHORT TO GROUND BLACK JACKS ARE GND, SO OK TO USE SCREW AND STANDARD WASHER.

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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.

Maximum Ratings
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

DISCLAIMER

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