

## Avionics RF Power LDMOS FET

The high power transistor part number ILD0912M15HV is designed for Avionics systems operating at 960-1215 MHz. Operating at 10 $\mu$ s, 10% pulse conditions this LDMOS FET device supplies a minimum of 15 watts of power at 960/1215 MHz. All devices are 100% screened for large signal RF parameters.



### Silicon LDMOS FET

- High Power Gain
- Superior thermal stability

### Class AB Operation

- Gate biased to  $I_{DQ} = 10$  mA

### Configuration

- Common Source

### Gold Metal

- Maximum Reliability

### Package

- Thermally enhanced
- Pb-free and RoHS-compliant

### Epoxy Sealed Lid

- Gross Leak Qualified

### RF Test Fixture

- Broadband
- Matched to 50 ohms
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

### PRELIMINARY DATA

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Lot/SN #:	Freq (MHz)	Pi (W)	Id (A)	RL (dB)	Po (W)	G (dB)	Nd' (%)	Droop (dB)	VSWR	
									2:1	20:1
WO: 50018426	960	0.8	1.06	9	24.4	14.84	50.8	-0.02	S	P
	1090	0.8	1.15	9	23.2	14.62	44.2	-0.04	S	P
	1215	0.8	1.02	9.4	21.8	14.35	47.4	-0.02	S	P

Vd=50V, Pulse = 10us-10%, Idq=10mA

Nd''= Dain Efficiency (excluding bias current)

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	$V_{DS}$	--	100	V	--
BD	Gate-Source Voltage	$V_{GS}$	--	20	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+200	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.24	°C/W	$V_D=50V, I_{DQ}=10mA, T_F=25\pm5^\circ C, P_{OUT}=15W$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

**DC ELECTRICAL CHARACTERISTICS**

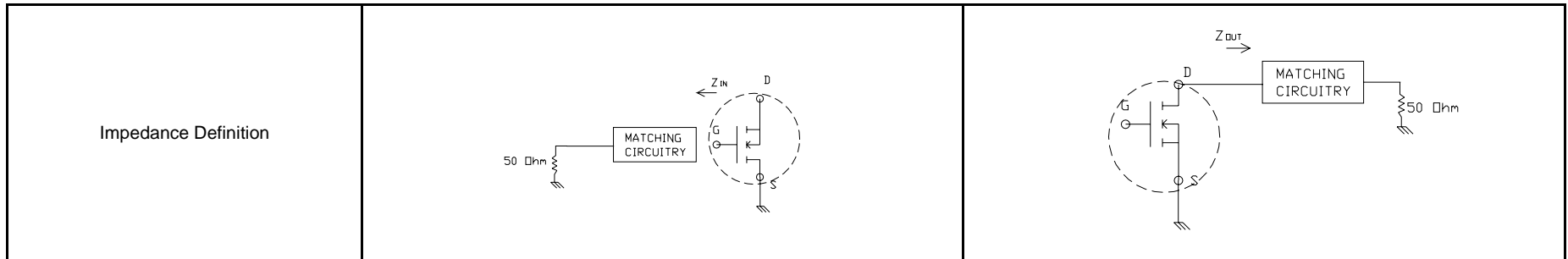
Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	$BV_{DSS}$	100		V	$I_D = 10mA, V_{GS} = 0V, T_F = 25\pm5^\circ C$
100%	Drain Leakage Current	$I_{DSS}$		5	$\mu A$	$V_{DS} = 50V, V_{GS} = 0V, T_F = 25\pm5^\circ C$
100%	Gate Threshold Voltage	$V_{GSTH2}$	2.5	4.0	V	$I_D = 10mA, T_F = 25\pm5^\circ C, V_{dd} = 50V$

**RF ELECTRICAL CHARACTERISTICS**

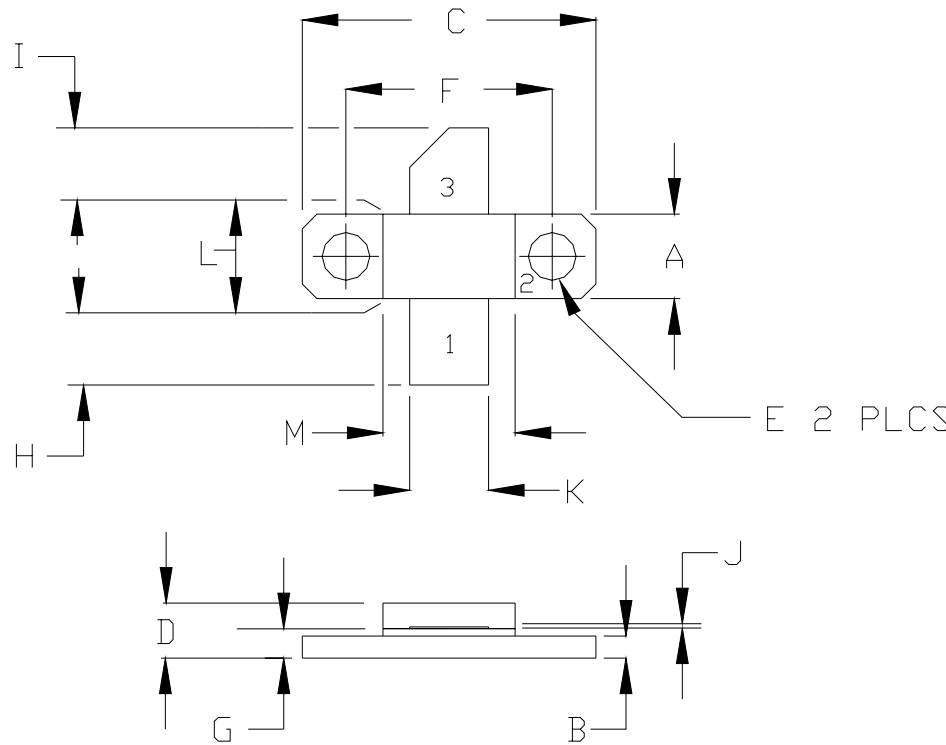
Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-7	dB	$V_{DD}=50V$ , $P_{IN}=0.8W$ , Pulse=10 $\mu$ s, 10%, $T_F=25\pm 5^\circ C$ , $F=F1$ , $I_{DQ}=10mA$ .
BD	Maximum Overdrive	$P_{IN(MAX)}$		1.5	W	$V_{DD}=50V$ , Pulse=10 $\mu$ s, 10%, $T_F=25\pm 5^\circ C$ , $F=F1$ , $I_{DQ}=10mA$ .
100%	Power Gain	$G_P$	12.73	15.23	dB	$V_{DD}=50V$ , $P_{IN}=0.8W$ , Pulse=10 $\mu$ s, 10%, $T_F=25\pm 5^\circ C$ , $F=F1$ , $I_{DQ}=10mA$ .
100%	Output Power	$P_{OUT}$	15	26.7	W	$V_{DD}=50V$ , $P_{IN}=0.8W$ , Pulse=10 $\mu$ s, 10%, $T_F=25\pm 5^\circ C$ , $F=F1$ , $I_{DQ}=10mA$ .
100%	Drain Current	$I_D$	1	2	A	$V_{DD}=50V$ , $P_{IN}=0.8W$ , Pulse=10 $\mu$ s, 10%, $T_F=25\pm 5^\circ C$ , $F=F1$ , $I_{DQ}=10mA$ .
100%	Drain Efficiency	$N_d'$	40	75	%	$V_{DD}=50V$ , $P_{IN}=0.8W$ , Pulse=10 $\mu$ s, 10%, $T_F=25\pm 5^\circ C$ , $F=F1$ , $I_{DQ}=10mA$ .
100%	Pulse Amplitude Droop	D	-0.5	0.5	dB	$V_{DD}=50V$ , $P_{IN}=0.8W$ , Pulse=10 $\mu$ s, 10%, $T_F=25\pm 5^\circ C$ , $F=F1$ , $I_{DQ}=10mA$ .
100%	Stability into 2:1 VSWR	VSWR-S			--	$V_{DD}=50V$ , $P_{IN}=0.8W$ , Pulse=10 $\mu$ s, 10%, $T_F=25\pm 5^\circ C$ , $F=F1$ , $I_{DQ}=10mA$ . Rotate 2:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
BD	Load Mismatch Tolerance	LMT	20:1		--	$V_{DD}=50V$ , $P_{IN}=0.8W$ , Pulse =10 $\mu$ s, 10%, $T_F=25\pm 5^\circ C$ , $F=F1$ , $I_{DQ}=10mA$ . Rotate 20:1 output VSWR through 360° phase. Survival.
BD	Pulse Risetime	RT		60	Ns	$V_{DD}=50V$ , $P_{IN}=0.8W$ , Pulse =10 $\mu$ s, 10%, $T_F=25\pm 5^\circ C$ , $F=F1$ , $I_{DQ}=10mA$ . Measure between 10% and 90% detected power points.
Note 1	F1 =960-1090-1215 MHz.					
Note 2	Pulse format = 10 $\mu$ s, 10%					
Note 3	$T_F$ = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (MHz)	$Z_{IF}$ ( $\Omega$ )	$Z_{OF}$ ( $\Omega$ )
960	1.00 -j0.36	4.50 +j11.0
1090	1.43 -j0.00	8.10 +j8.90
1215	1.40 -j.030	5.60 +j9.50



**PACKAGE DIMENSIONAL OUTLINE DRAWING**

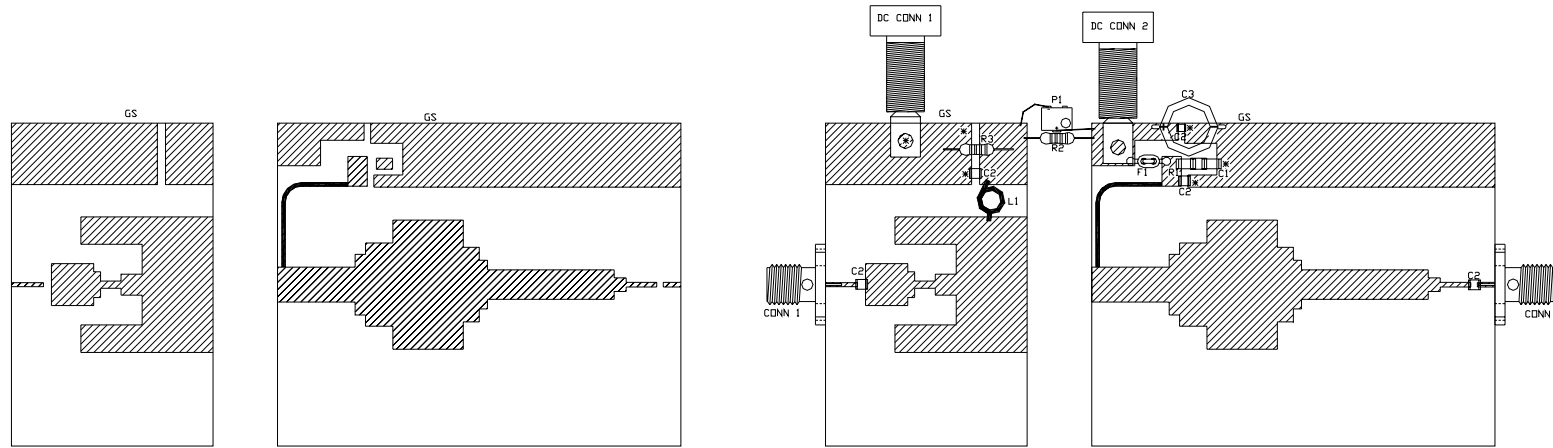


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.077	0.087	1.95	2.20
H	0.215	0.245	5.46	6.22
I	0.215	0.245	5.46	6.22
J	0.004	0.006	0.10	0.15
K	0.210	0.220	5.33	5.58
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN SCHEDULE	
1	GATE
2	SOURCE
3	DRAIN

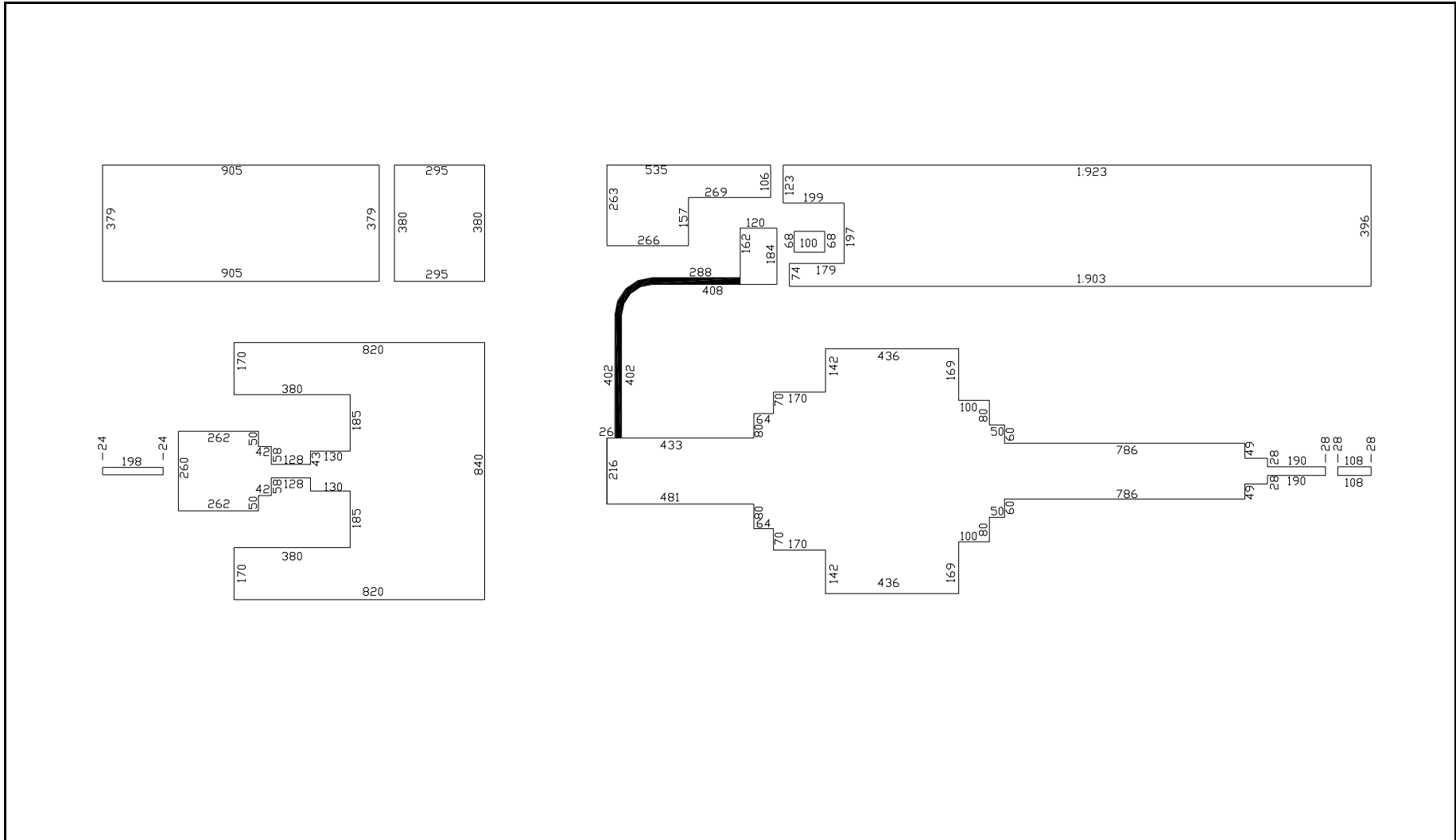
NOTES:  
LID: LID-PL32-1

**RF TEST FIXTURE – ASSEMBLY AND PARTS LIST**

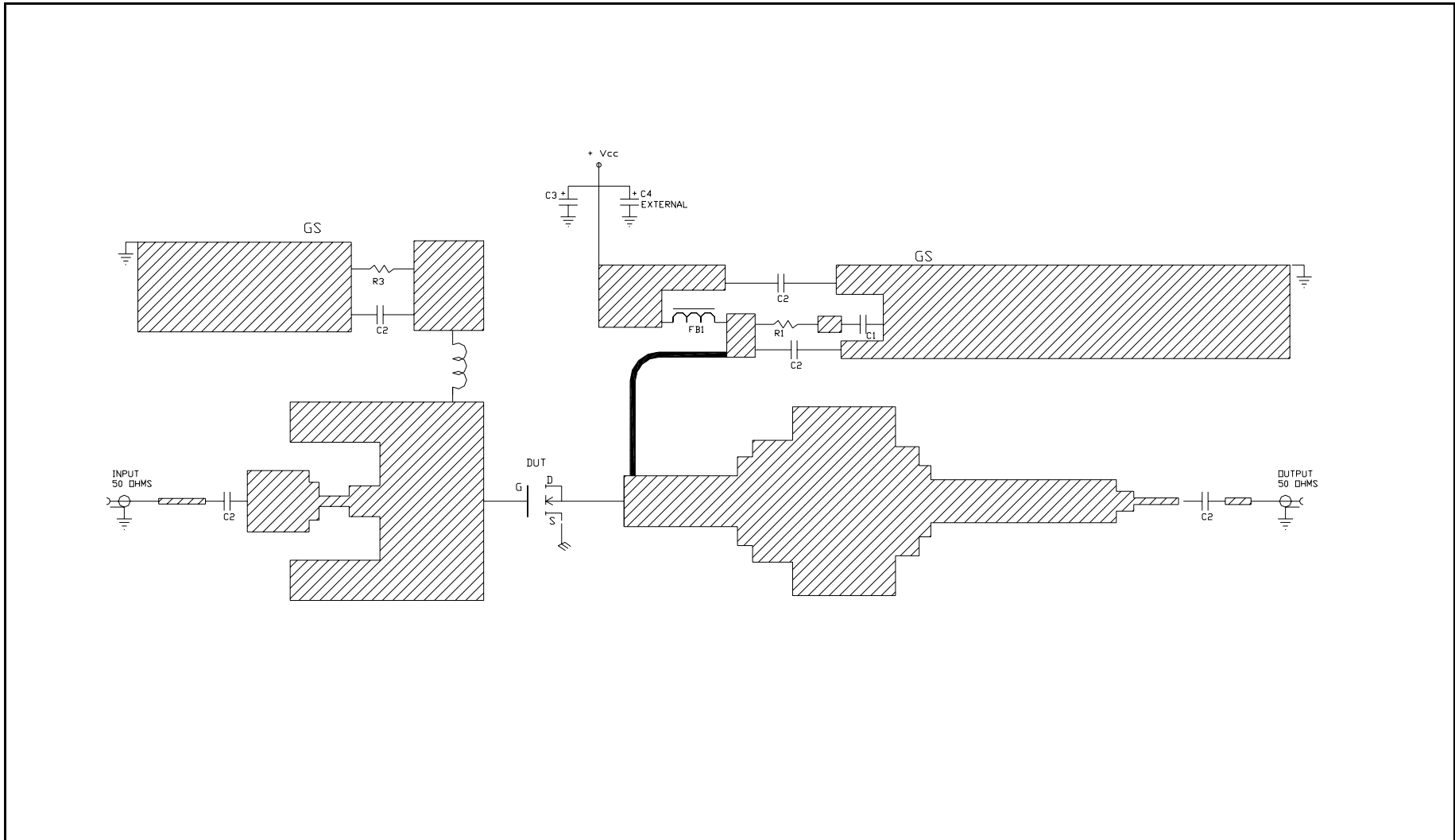


COMPONENT	DESCRIPTION
DUT	TRANSISTOR #ILD0912M15HV MOUNT HARD TO THE RIGHT
PC BOARD	RODGERS #RT6010.2LM 2E/2E .025"
C1	CHIP CAPACITOR ATC00A (C1) - 0.1uF
C2	CHIP CAPACITOR ATC100A (C2) - 100pF
C3	ELECTROLYTIC CAPACITOR 68uF
C4 (NOT SHOWN)	ELECTROLYTIC CAPACITOR 4700uF / 50V
R1	SNUB RESISTOR 6.8I OHMS
R2	RESISTOR 10K OHMS
R3	RESISTOR 560 OHMS
L1	TURNS # 18 AWG, 0.125" DIA, 0.18" LONG PULL TIGHT AND FULLY CLOSED, LEFT HAND.
R4	RESISTOR 1 M OHMS
P1	PROBETIDMETER
F1	BIAS WIRE WITH FERRITE BEAD
GS (2 PLACES)	GROUND SHIM, COPPER, TH=0.001"
CONN 1, CONN 2	SMA CONNECTOR, DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-04 (1.25")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-06 (1.75")
TRANSISTOR CARRIER	2 INCH COPPER-05 (PL32)
TRANSISTOR CLAMP	NUTR1 CLAMP-07
ALUMINUM HEAT SINK	2 INCH HEATSINK-09
DC CONN 1	BANANA JACK, BLACK
DC CONN 2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

**RF TEST FIXTURE – CIRCUIT DIMENSIONS IN MILS**



**RF TEST FIXTURE – ELECTRICAL SCHEMATIC**



**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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