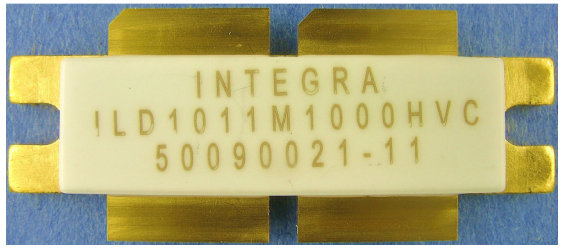
Part Number: ILD1011M1000HVC

Integra
TECHNOLOGIES, INC.

Avionics Band RF Power LDMOS FET

The high power transistor part number ILD1011M1000HVC is designed for Avionics systems operating at 1030 MHz. Operating at 50µs, 2% pulse conditions this LDMOS FET device supplies a minimum of 1000 watts of power at 1030 MHz. All devices are 100% screened for large signal RF parameters.



Silicon LDMOS FET
- High Power Gain
- Superior thermal stability

Class AB Operation
- Gate biased to I_{DQ} = 60 mA

Configuration
- Common Source

Gold Metal
- Maximum Reliability

Package
- Thermally enhanced
- Pb-free and RoHS-compliant

Epoxy Sealed Lid
- Gross Leak Qualified

RF Test Fixture
- Broadband
- Matched to 50 ohms
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

TYPICAL DATA ***TYPICAL DATA*** ***TYPICAL DATA*** ***TYPICAL DATA***

Lot/SN	Freq (MHz)	P_I (W)	I_D (A)	RL (dB)	P_O (W)	Nd' (%)	G (dB)	VSWR 2:1	VSWR 3:1
50027723-1	1030	20	38.55	14	1085	59.4	17.34	S	P

Pulse format = 50µs, 2% I_{DQ} = 60mA, Vd=50V

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MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	92	V	--
BD	Gate-Source Voltage	V_{GS}	--	20	V	--
BD	Storage Temperature Range	T_{STG}	-55	+200	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	TBD	°C/W	V_D=50V, I_{DQ}=60mA, T_F=25±5°C, P_{OUT}=1000W
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	92	--	V	I_D = 70mA, V_{GS} = 0V, T_F = 25±5°C
100%	Drain Leakage Current	I_{DSS}	--	48	µA	V_{DS} = 50V, V_{GS} = 0V, T_F = 25±5°C
100%	Gate Threshold Voltage	V_{GSTH2}	2.75	5.25	V	I_D = 100mA, T_F = 25±5°C, V_{DS} = 5V
100%	Gate Leakage Current	I_{GSS}	--	1	µA	V_{GS} = 5V, V_{DS} = 0V, T_F = 25±5°C

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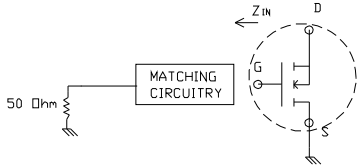
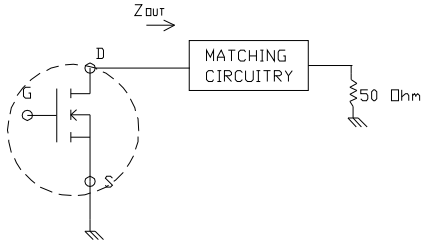
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	10	--	dB	V_{DD}=50V, P_{in}=20W, Pulse=50µs, 2%, T_F=25±5°C, F=F1, I_{DQ}=60mA.
BD	Maximum Overdrive	$P_{IN(MAX)}$	--	28	W	V_{DD}=50V, Pulse=50µs, 2%, T_F=25±5°C, F=F1, I_{DQ}=60mA.
100%	Power Gain	G_P	16.99	18.49	dB	V_{DD}=50V, P_{in}=20W, Pulse=50µs, 2%, T_F=25±5ºC, F=F1, I_{DQ}=60mA.
100%	Output Power	Pout	1000	1416	W	V_{DD}=50V, P_{in}=20W, Pulse=50µs, 2%, T_F=25±5ºC, F=F1, I_{DQ}=60mA.
100%	Drain Efficiency	N'_d	45	75	%	V_{DD}=50V, P_{in}=20W, Pulse=50µs, 2%, T_F=25±5°C, F=F1, I_{DQ}=60mA.
100%	Pulse Amplitude Droop	D	-0.5	+0.5	dB	V_{DD}=50V, P_{in}=20W, Pulse=50µs, 2%, T_F=25±5°C, F=F1, I_{DQ}=60mA.
100%	Stability into 2:1 VSWR	VSWR-S		2:1	--	V_{DD}=50V, P_{in}=20W, Pulse=50µs, 2%, T_F=25±5°C, F=F1, I_{DQ}=60mA. Rotate 2:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	Load Mismatch Tolerance Limit	LMT		3:1	--	V_{DD}=50V, P_{in}=20W, Pulse=50µs, 2%, T_F=25±5°C, F=F1, I_{DQ}=60mA. Rotate 3:1 output VSWR through 360° phase. Survival.
BD	Load Mismatch Tolerance	LMT		20:1	--	V_{DD}=50V, P_{in}=20W, Pulse=50µs, 2%, T_F=25±5°C, F=F1, I_{DQ}=60mA. Rotate 20:1 output VSWR through 360° phase. Survival.
BD	Pulse Risetime	RT		60	ns	V_{DD}=50V, P_{in}=20W, Pulse=50µs, 2%, T_F=25±5°C, F=F1, I_{DQ}=60mA. Measure between 10% and 90% detected power points.

Note 1	F1 = 1030MHz.
Note 2	Pulse format = 50µs, 2%
Note 3	T_F = Device flange temperature.
Note 4	Screen 'BD' = parameter qualified By Design.

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (MHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
1030	0.81+j1.14	0.87+j1.88
Impedance Definition		

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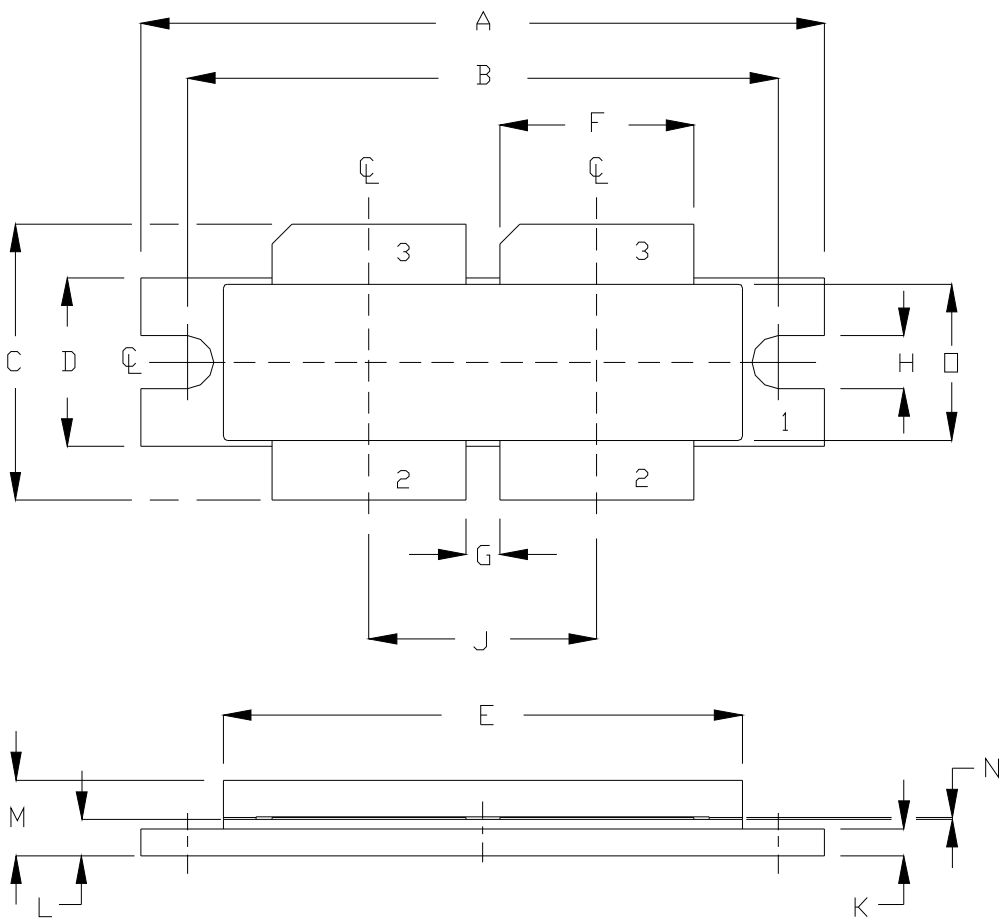
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.27
B	1.395	1.405	35.43	35.69
C	0.634	0.674	16.10	17.12
D	0.395	0.405	10.03	10.29
E	1.219	1.241	30.96	31.52
F	0.455	0.465	11.56	11.81
G	0.075	0.085	1.90	2.16
H	0.120	0.130	3.05	3.30
J	0.535	0.545	13.59	13.84
K	0.059	0.069	14.99	17.53
L	0.081	0.091	2.06	2.31
M	0.164	0.194	4.16	4.93
N	0.004	0.007	0.10	0.18
□	0.354	0.364	8.99	9.24

PIN	SCHEDULE
1	SOURCE
2	GATE
3	DRAIN

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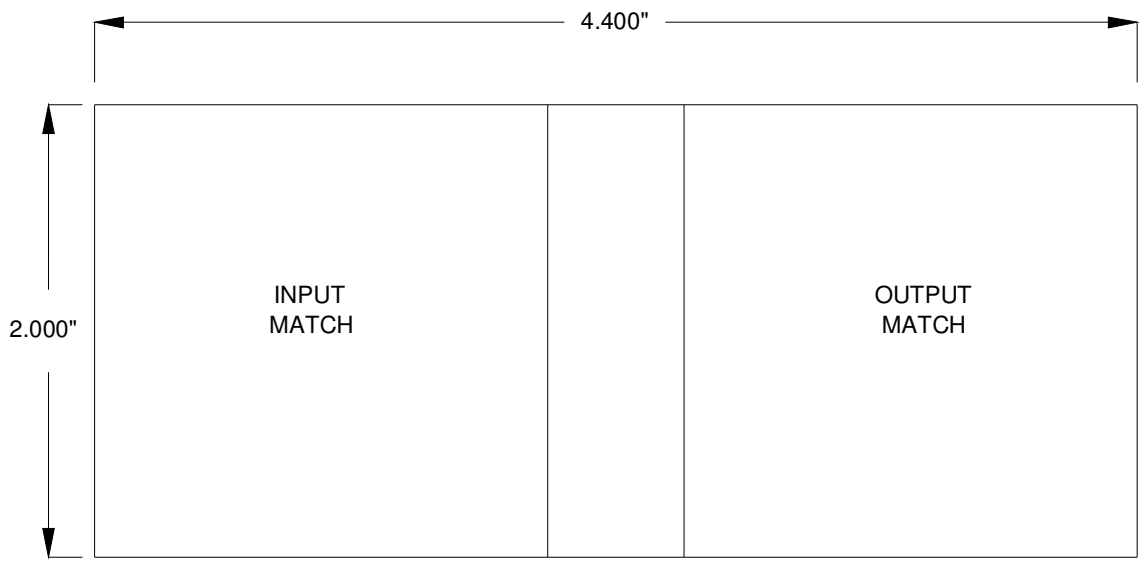
RF TEST FIXTURE



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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