

**Avionics Band RF Power LDMOS FET**

The high power transistor part number ILD1011M30 is designed for Avionics systems operating at 1030-1090 MHz. This LDMOS FET device under 50us, 2% pulse format supplies a minimum of 30 watt of peak pulse power. All devices are 100% screened for large signal parameters.



**Silicon LDMOS FET**

- High Power Gain
- Superior thermal stability
- Gold Metal

**Class AB Operation**

- Gate biased to  $I_{DQ}=10mA$

**Configuration**

- Common Source

**Gold Metal**

- Maximum Reliability

**BeO - Free Package**

- Metal Based
- Epoxy Seal

**Epoxy Sealed Lid**

- Gross Leak Qualified

**RF Test Fixture**

- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed

*TYPICAL DATA    TYPICAL DATA    TYPICAL DATA    TYPICAL DATA*

Freq (GHz)	PW (us)	Duty (%)	V <sub>DS</sub> (V)	P <sub>IN</sub> (W)	IRL (dB)	P <sub>out</sub> (W)	G <sub>p</sub> (dB)	I <sub>D</sub> (A)	VSWR 3:1
1.030	50	2	28.0	1	14	46.3	16.66	3.50	P
1.090	50	2	28.0	1	13	40.3	16.05	2.75	P

$I_{DQ}=10mA$

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	$V_{DS}$	--	62	V	--
BD	Gate-Source Voltage	$V_{GS}$	-0.5	12	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.17	°C/W	$V_{DS}=28V, I_{DQ}=10mA, T_F=25\pm 5^\circ C, P_{IN}=1W$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

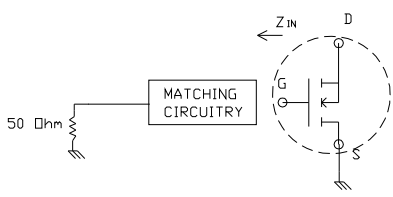
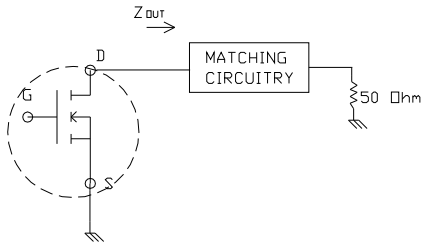
**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	$BV_{DSS}$	62	--	V	$I_{DS}=20mA, V_{GS}=0V, T_F=25\pm 5^\circ C.$
100%	Drain Leakage Current	$I_{DSS}$	--	3	uA	$V_{DS}=28V, V_{GS}=0V, T_F=25\pm 5^\circ C.$
100%	Operating Gate Voltage	$V_{GS}$	2.75	4.75	V	$I_{DS}=100mA, V_{DS}=5V, T_F=25\pm 5^\circ C.$
100%	Gate Leakage Current	$I_{GSS}$	--	1.0	uA	$V_{GS}=5V, V_{DS}=0V, T_F=25\pm 5^\circ C.$

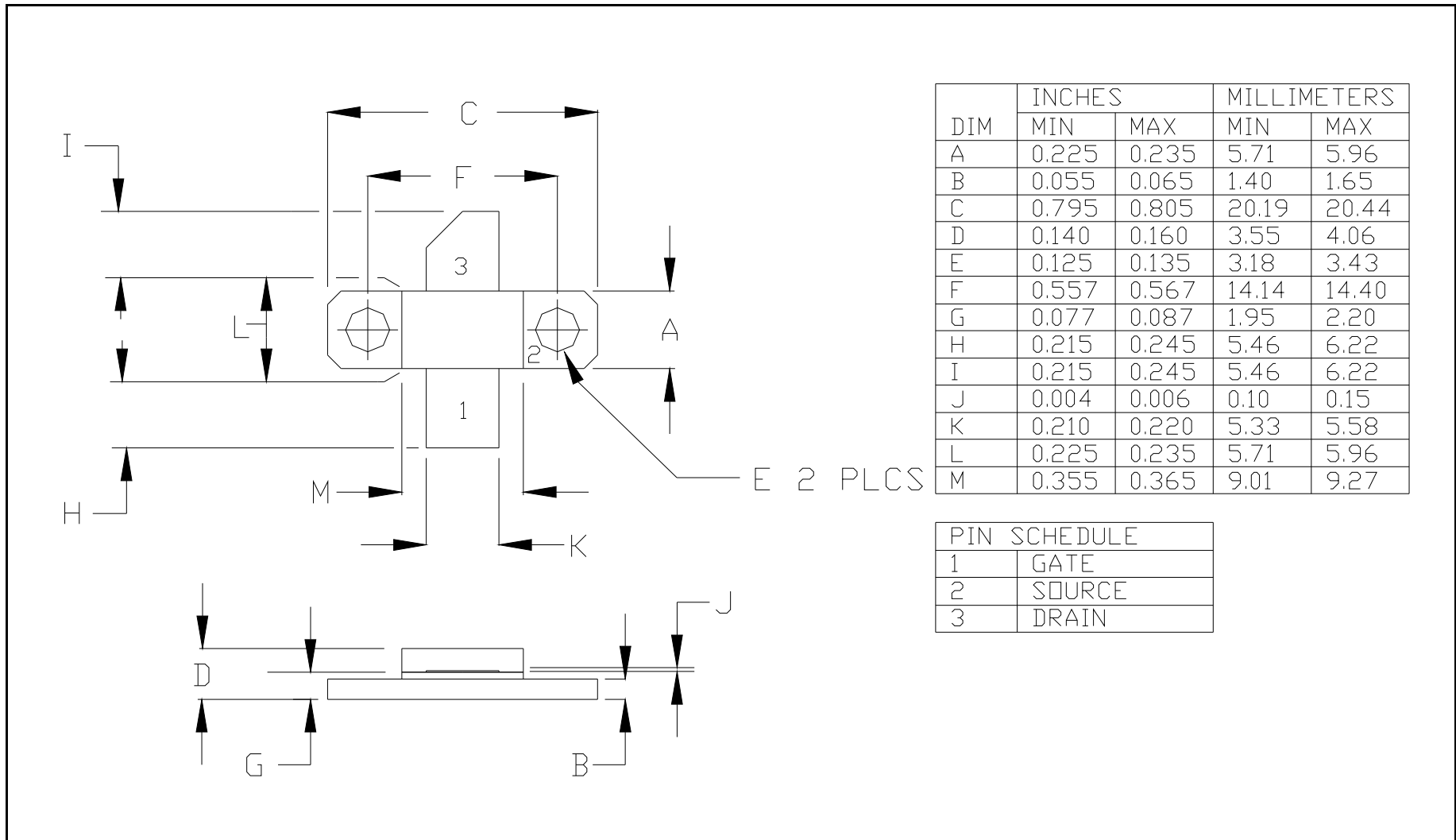
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-10	dB	$V_{DS}=28V$ , $P_{in}=1W$ , Pulse=PW1 @ F1, F2, $T_F=25\pm5^\circ C$ , $I_{DQ}=10mA$ .
100%	Drain Efficiency	Nd	40	80	%	$V_{DS}=28V$ , $P_{in}=1W$ , Pulse=PW1 @ F1, F2, $T_F=25\pm5^\circ C$ , $I_{DQ}=10mA$ .
100%	Power Gain	Gp	14.77	20.00	dB	$V_{DS}=28V$ , $P_{in}=1W$ , Pulse=PW1 @ F1, F2, $T_F=25\pm5^\circ C$ , $I_{DQ}=10mA$ .
100%	Output Power	Pout	30	100	W	$V_{DS}=28V$ , $P_{in}=1W$ , Pulse=PW1 @ F1, F2, $T_F=25\pm5^\circ C$ , $I_{DQ}=10mA$ .
100%	Stability into 1.5:1 VSWR	VSWR-S	--	3:1	--	$V_{DS}=28V$ , $P_{in}=1W$ , Pulse=PW1 @ F1, F2, $T_F=25\pm5^\circ C$ , $I_{DQ}=10mA$ Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	Load Mismatch Tolerance	LMT	--	3:1	--	$V_{DS}=28V$ , $P_{in}=1W$ , Pulse=PW1 @ F1, F2, $T_F=25\pm5^\circ C$ , $I_{DQ}=10mA$ , Rotate 3:1 output VSWR through 360° phase.
Note 1	F1=1030 MHz, F2=1090 MHz.					
Note 2	Pulse format: PW1= 50us, 2%					
Note 3	$T_F$ = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

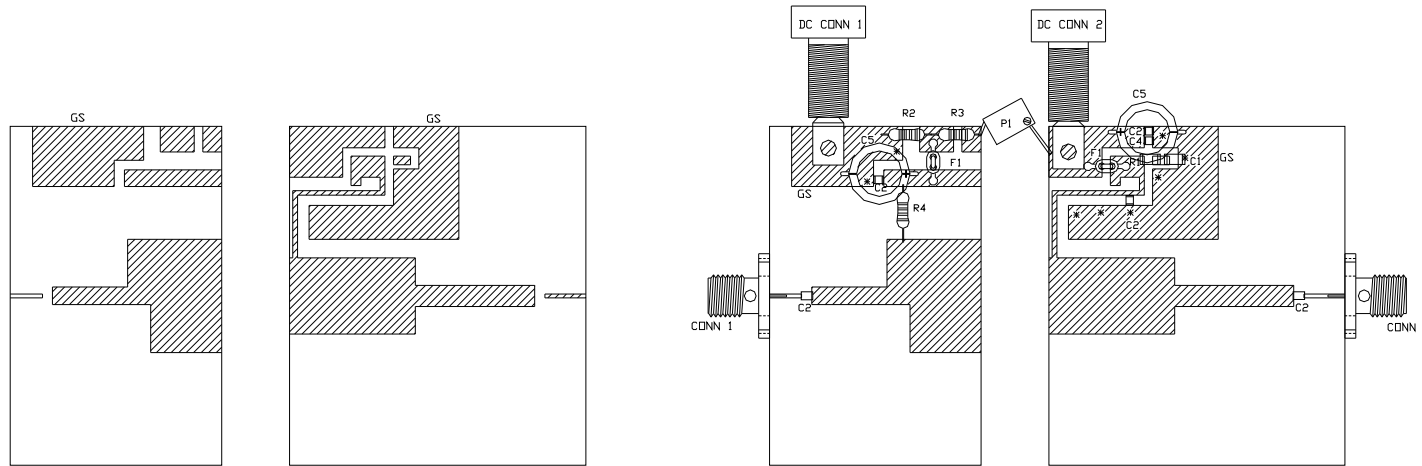
**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (MHz)	$Z_{IF}$ ( $\Omega$ )	$Z_{OF}$ ( $\Omega$ )
1030	1.20 -j1.51	2.84 +j1.18
1090	1.21 -j1.24	3.33 +j1.48
Impedance Definition		

**PACKAGE DIMENSIONAL OUTLINE DRAWING**



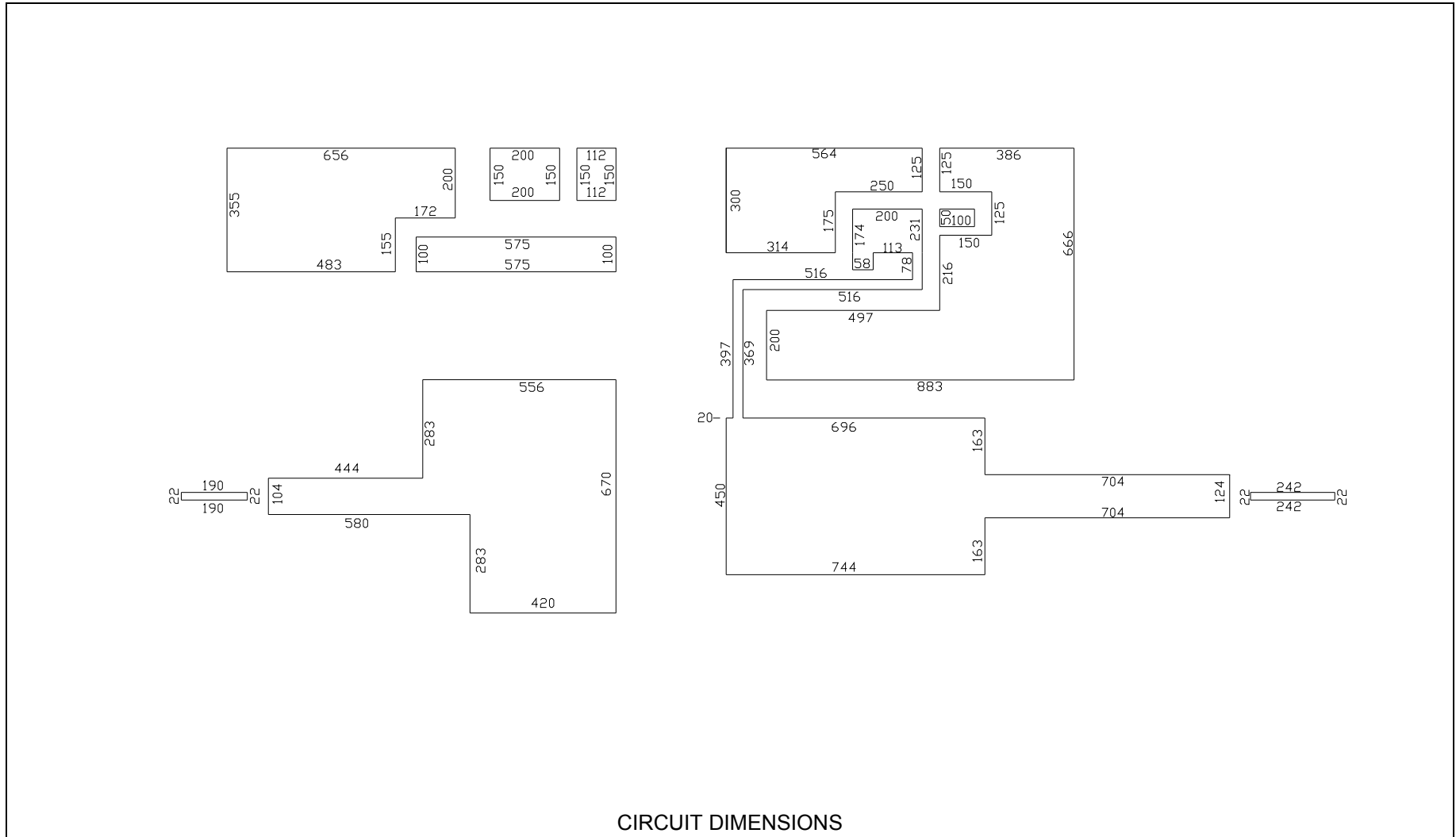
**RF TEST FIXTURE**



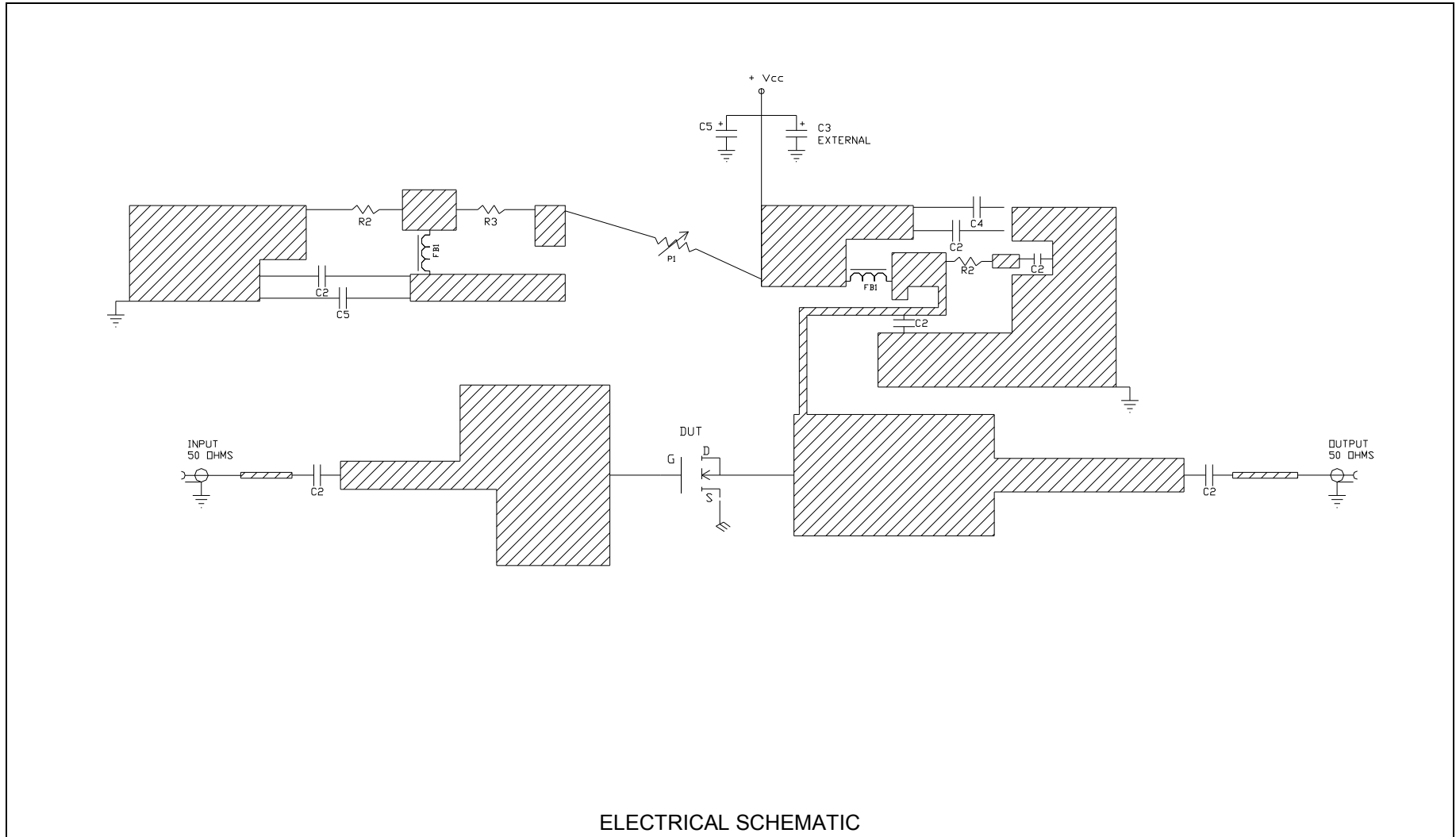
COMPONENT	DESCRIPTION
DUT	TRANSISTOR #ILD1011M30 MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #R06010.2LM 2E/2E .025"
C1	SNUB CAPACITOR 0.1uF
C2	CHIP CAPACITOR ATC100A 100pF
C3 (NOT SHOWN)	ELECTROLYTIC CAPACITOR, 4700uF / 50V
C4	CHIP CAPACITOR ATC100A 4.7uF
C5, C5	ELECTROLYTIC CAPACITOR 68uF
R1	SNUB RESISTOR 6.81 OHMS
R2	RESISTOR 12 K OHMS
R3	RESISTOR 68 K OHMS
R4	RESISTOR 1 M OHMS
F1	BIAS WITH FERRITE BEAD
P1	POTENTIOMETER 100KOHMS
GS (8 PLACES)	GROUND SHIM, COPPER, TH=0.001"
CONN 1, CONN 2	SMA CONNECTOR, DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-04 (1.25")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-06 (1.75")
TRANSISTOR CARRIER	2 INCH COPPER-07 (PL32)
TRANSISTOR CLAMP	NORYL CLAMP-07
ALUMINUM HEAT SINK	2 INCH HEATSINK-09
DC CONN 1	BANANA JACK, BLACK
DC CONN 2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

**ASSEMBLY AND PARTS LIST**

**RF TEST FIXTURE**



**RF TEST FIXTURE**



ELECTRICAL SCHEMATIC

**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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