

Part Number: **ILD1214M10 (Preliminary)**

Integra

TECHNOLOGIES, INC.

Avionics Band RF Power LDMOS FET

The high power transistor part number ILD1214M10 is designed for L-Band radar operating at 1200-1400 MHz. This LDMOS FET device under 300us, 10% pulse format supplies a minimum of 10-15 watt of peak pulse power. All devices are 100% screened for large signal parameters.



Silicon LDMOS FET

- High Power Gain
- Superior thermal stability
- Gold Metal

Class AB Operation

- Gate biased to $I_{DQ}=10\text{mA}$

Configuration

- Common Source

Gold Metal

- Maximum Reliability

BeO - Free Package

- Metal Based
- Epoxy Seal

Epoxy Sealed Lid

- Gross Leak Qualified

RF Test Fixture

- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed

PRELIMINARY DATA

PRELIMINARY DATA

PRELIMINARY DATA

General Information ILD1214M10	Test Sequence Name	Freq (MHz)	PIN (W)	RL (dB)	POUT (W)	GP (dB)	dG (dB)	Id (A)	nd (%)	Droop (dB)	VSWR-S 1.5:1 (P-F)	VSWR-LMT 2:1 (P-F)
Date: 5/8/2009												
Assbly Lot - SN : TBD	Nominal	1200	1	-13.0	20	13.08		1.620	41.8	-0.40	P	P
Wafer : TBD												
Test Fixture : NA	Nominal	1300	1	-18.0	22	13.42	0.41	1.480	49.5	-0.26	P	P
Pass / Fail : Device Passes												
OPERATOR: FB	Nominal	1400	1	-11.0	20	13.01		1.250	53.3	-0.14	P	P
Pulse:300us-10% Vd=30V, Idq=10mA												

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	TBD	°C/W	$V_{DS}=28V, I_{DQ}=10mA, T_F=25\pm5^\circ C, P_{IN}=1W$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	$I_{DS}=10\mu A, V_{GS}=0V, T_F=25\pm5^\circ C.$
100%	Drain Leakage Current	I_{DSS}	--	1.0	uA	$V_{DS}=28V, V_{GS}=0V, T_F=25\pm5^\circ C.$
100%	Operating Gate Voltage	V_{GS}	2.5	4.0	V	$V_{DS}=28V, T_F=25\pm5^\circ C.$
100%	Gate Leakage Current	I_{GSS}	--	1.0	uA	$V_{GS}=10V, V_{DS}=0V, T_F=25\pm5^\circ C.$

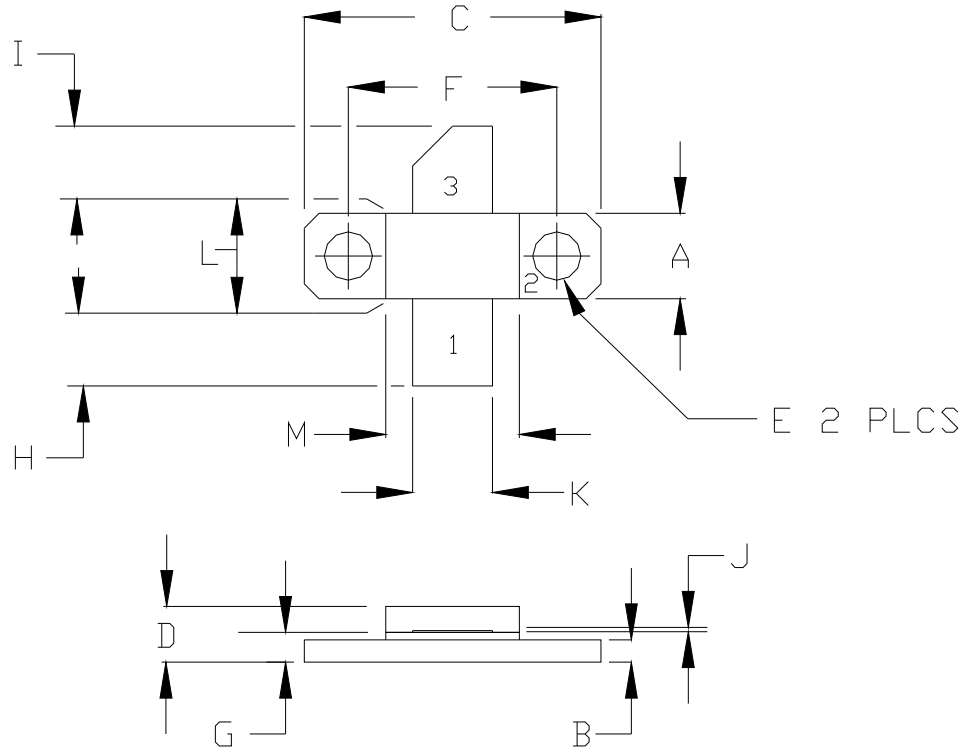
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-7	dB	$V_D=30V$, $P_{in}=1W$, Pulse= $PW1$ @ F1, F2, F3, $T_F=25\pm5^\circ C$, $I_{DQ}=10mA$.
100%	Drain Efficiency	Nd	30	75	%	$V_D=30V$, $P_{in}=1W$, Pulse= $PW1$ @ F1, F2, F3, $T_F=25\pm5^\circ C$, $I_{DQ}=10mA$.
100%	Power Gain	Gp	10	--	dB	$V_D=30V$, $P_{in}=1W$, Pulse= $PW1$ @ F1, F2, F3, $T_F=25\pm5^\circ C$, $I_{DQ}=10mA$.
100%	Output Power	Pout	10	--	W	$V_D=30V$, $P_{in}=1W$, Pulse= $PW1$ @ F1, F2, F3, $T_F=25\pm5^\circ C$, $I_{DQ}=10mA$.
100%	Signal Amplitude Droop	Droop	-0.5	0.5	dB	$V_D=30V$, $P_{in}=1W$, Pulse= $PW1$ @ F1, F2, F3, $T_F=25\pm5^\circ C$, $I_{DQ}=10mA$.
100%	Stability into 1.5:1 VSWR	VSWR-S	1.5:1	--	--	$V_D=30V$, $P_{in}=1W$, Pulse= $PW1$ @ F1, F2, F3, $T_F=25\pm5^\circ C$, $I_{DQ}=10mA$ Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	Load Mismatch Tolerance	VSWR-LMT	2:1	--	--	$V_D=30V$, $P_{in}=1W$, Pulse= $PW1$ @ F1, F2, F3, $T_F=25\pm5^\circ C$, $I_{DQ}=10mA$, Rotate 2:1 output VSWR through 360° phase.
Note 1	F1=1200 MHz, F2=1300 MHz, F3=1400 MHz					
Note 2	Pulse format: PW1= 300us, 10%					
Note 3	T_F = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

OPTIMAL IMPEDANCE CHARACTERISTICS

Frequency (MHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
1200	3.1 -j3.2	15 -j2.9
1300	3.3 -j4.6	12.1 -j 2
1400	3.5 -j 5	10 +j4.4
Impedance Definition		

PACKAGE DIMENSIONAL OUTLINE DRAWING

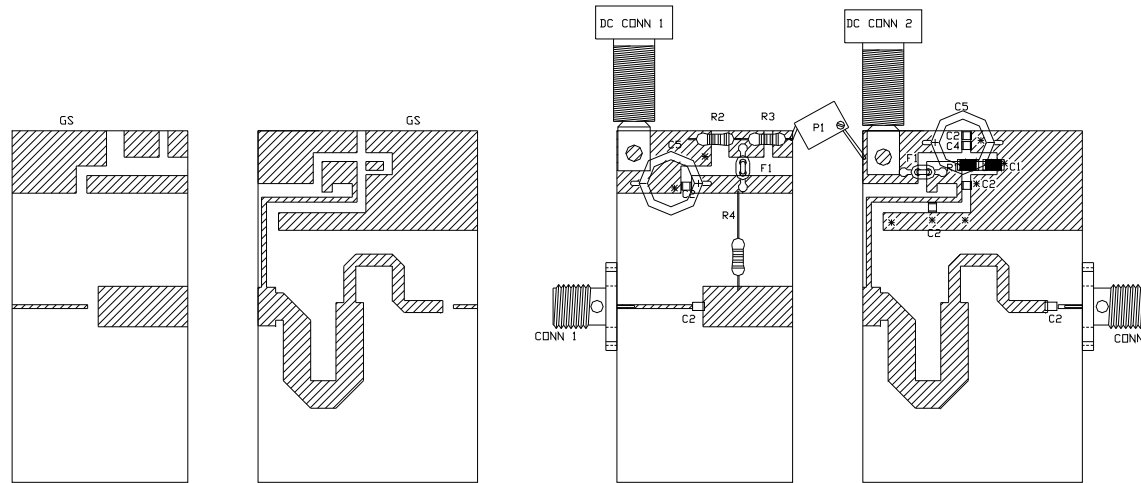


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.077	0.087	1.95	2.20
H	0.050	0.070	1.27	1.77
I	0.215	0.245	5.46	6.22
J	0.215	0.245	5.46	6.22
K	0.210	0.220	5.33	5.58
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN SCHEDULE	
1	GATE
2	SOURCE
3	DRAIN

NOTES:
LID: LID-PL32-1

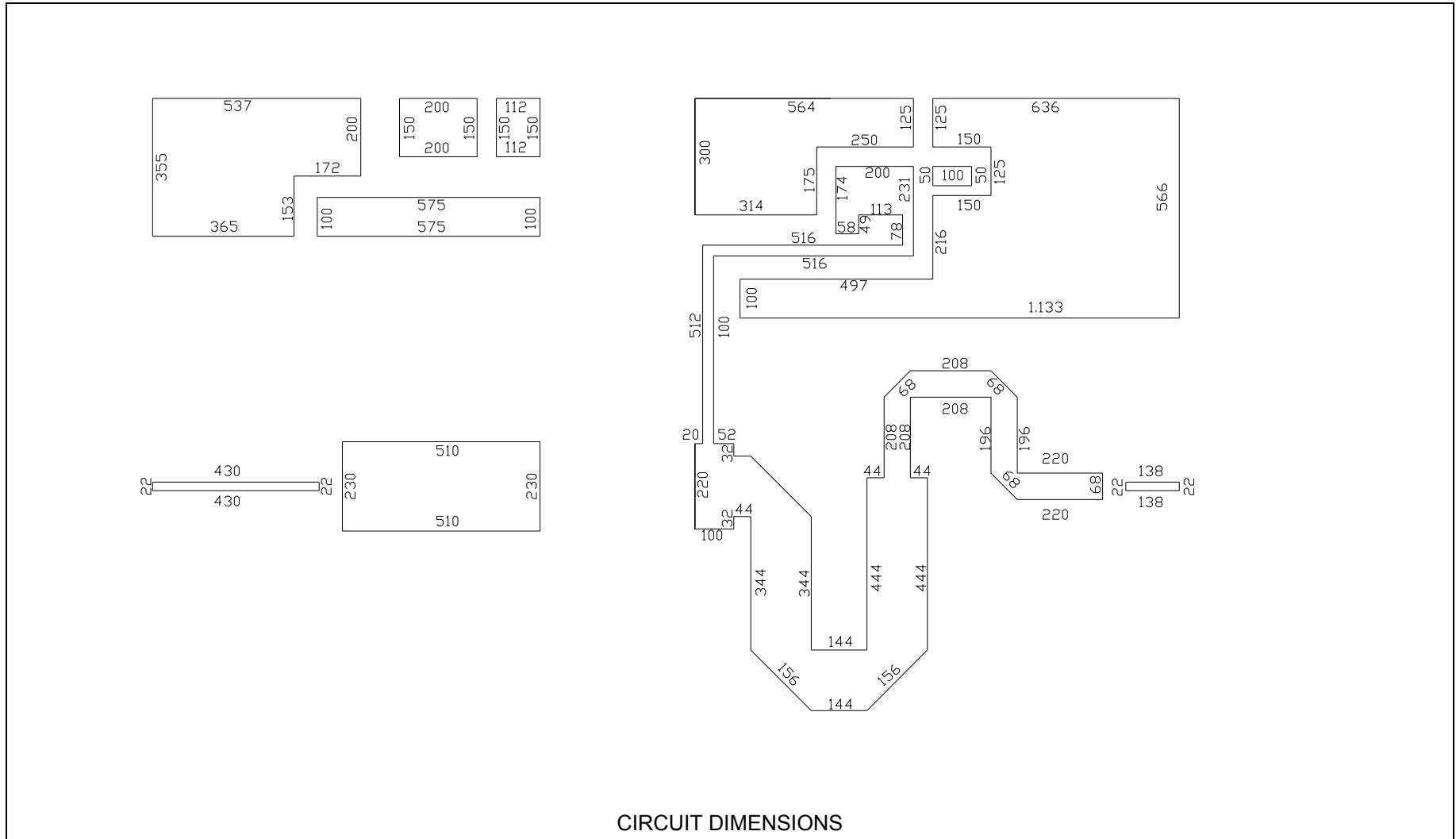
RF TEST FIXTURE



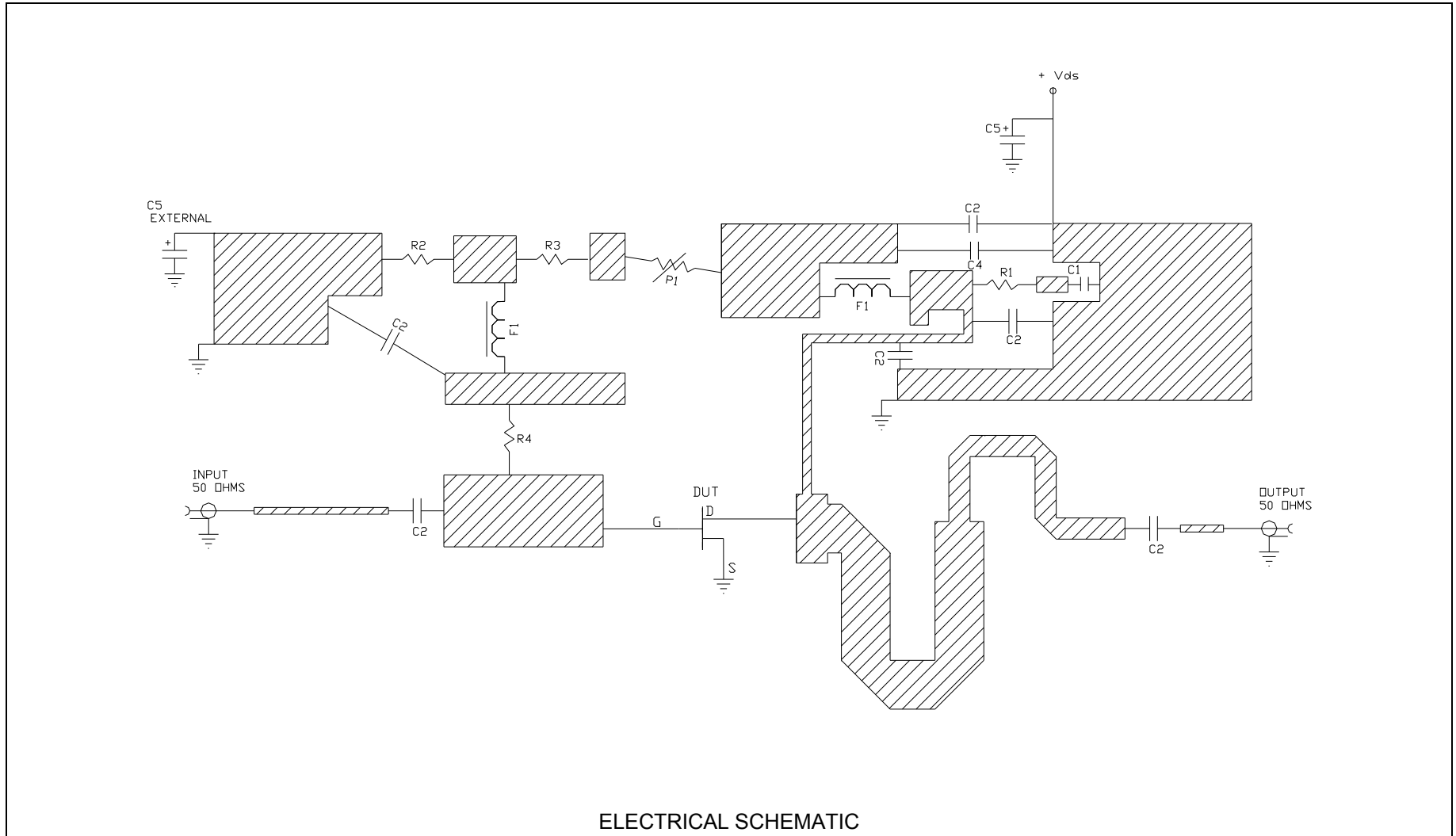
COMPONENT	DESCRIPTION
DUT	TRANSISTOR #ILD1214M10 MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RT6010.2LM 2E/2E .025"
C1	SNUB CAPACITOR .01uF
C2	CHIP CAPACITOR ATC100A 100pF
C4	CHIP CAPACITOR ATC100A 4.7uF
C5 (NOT SHOWN)	ELECTROLYTIC CAPACITOR 68uF
R1	SNUB RESISTOR 6.810HMS
R2	RESISTOR 12 K OHMS
R3	RESISTOR 68 K OHMS
R4	1 M OHMS
F1	BIASWIRE WITH TWIN CORE FERRITE BEAD
P1	POTENTIOMETER 100 K OHMS
GS (8 PLACES)	GROUND SHIM COPPER, TH=0.001"
CONN 1, CONN 2	SMA CONNECTOR, DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-03 (1")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-04 (1.25")
TRANSISTOR CARRIER	2 INCH COPPER-01
TRANSISTOR CLAMP	NDRYL CLAMP-01
ALUMINUM HEAT SINK	2 INCH HEAT-SINK-01
DC CONN 1	BANANA JACK, BLACK
DC CONN 2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

ASSEMBLY AND PARTS LIST

RF TEST FIXTURE



RF TEST FIXTURE



ELECTRICAL SCHEMATIC

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

DISCLAIMER

Integra Technologies Inc. reserves the right to make changes without further notice to any products herein. Integra Technologies Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Integra Technologies Inc. assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Integra Technologies Inc. products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integra Technologies Inc. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integra Technologies Inc. for any damages resulting from such improper use or sale.