

S-Band RF Power LDMOS Transistor

The high power pulsed transistor part number ILD2326M200 is designed for S-Band systems operating at 2.25–2.55 GHz. Operating at a pulse width of 0.5ms with a duty factor of 17%, this dual MOSFET device supplies a minimum of 200 watts of peak pulse power across the instantaneous operating bandwidth of 2.25-2.55 GHz. Fabricated with all gold metal contact, wire bonding and package for maximum reliability. All devices are 100% screened for large signal RF parameters in the broadband RF test fixture across the entire specified operating bandwidth with no variable or external tuning.



Silicon LDMOS

- High Power Gain
- Superior thermal stability

Class AB Operation

- Gate biased to $I_{DQ}=2 \times 40\text{mA}$

Configuration

- Common Source

Gold Metal

- Gold Chip Metal
- Gold Wire Bond
- Maximum Reliability

Package

- Thermally Enhanced
- Gold Metal based

Epoxy Sealed Lid

- Gross Leak Qualified

RF Test Fixture

- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

TYPICAL DATA

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Device	Bias (mA)	Freq (MHz)	PW (ms)	Duty (%)	V _{DD} (V)	P _{IN} (W)	IRL (dB)	P _{OUT} (W)	G _p (dB)	I _d (A)	η _D (%)	Drp (dB)	VSWR 1.5:1	VSWR 2:1
50022385-1	80	2250	0.5	17	28	24	-18	215	9.5	18.9	41	-0.24	P	P
	80	2400	0.5	17	28	24	-17	229	9.8	19.4	42	-0.28	P	P
	80	2550	0.5	17	28	24	-16	208	9.4	16.8	44	-0.33	P	P

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	70	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	+12	V	--
BD	Storage Temperature Range	T_{STG}	-40	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
BD	CW Power	P_{CW}	--	200	W	--
Note Screen 'BD' = parameter qualified By Design.						

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.10	°C/W	V1, I_{DQ1} , T_{F1} , PW1, DF1.
Note Screen 'BD' = parameter qualified By Design.						

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.						
Note Screen 'LM' = parameter is qualified by assembly line monitor.						

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage (each side)	BV_{DSS}	65	--	V	$I_D = 10mA$, $V_{GS} = 0V$, $T_F = 25 \pm 5^\circ C$
100%	Drain Leakage Current (each side)	I_{DSS}	--	1.0	μA	$V_{DS} = 28V$, $V_{GS} = 0V$, $T_F = 25 \pm 5^\circ C$
100%	Gate Threshold Voltage (each side)	V_{GSTH2}	1.5	3.0	V	$I_D = 0.1A$, $V_{DS} = 5V$, $T_F = 25 \pm 5^\circ C$
100%	Gate Leakage Current (each side)	I_{GSS}	--	1.0	μA	$V_{GS} = 5V$, $V_{DS} = 0V$, $T_F = 25 \pm 5^\circ C$

RF ELECTRICAL CHARACTERISTICS

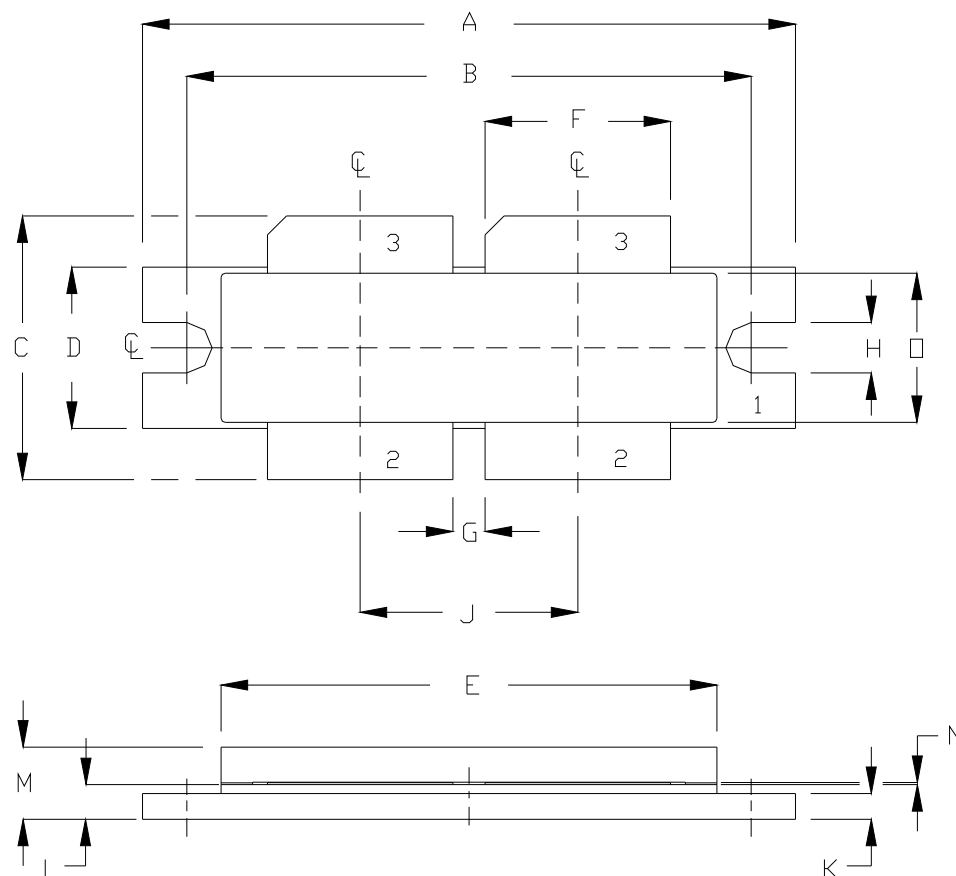
Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-10	dB	$V_{DD}=V_1$; $I_{DQ}=I_{DQ1}$; $T_F=T_{F1}$; $P_O=P_{OUT1}$; $F=F_1, F_2, F_3$: PW1,DF1
100%	Output Power	P_{OUT}	200	317	W	$V_{DD}=V_1$; $I_{DQ}=I_{DQ1}$; $T_F=T_{F1}$; $F=F_1, F_2, F_3$: PW1,DF1
100%	Power Gain	G_P	9.21	11.21	dB	$V_{DD}=V_1$; $I_{DQ}=I_{DQ1}$; $T_F=T_{F1}$; $P_O=P_{OUT1}$; $F=F_1, F_2, F_3$: PW1,DF1
100%	Pulse Amplitude Droop	Drp	-0.5	0.5	dB	$V_{DD}=V_1$; $I_{DQ}=I_{DQ1}$; $T_F=T_{F1}$; $P_O=P_{OUT1}$; $F=F_1, F_2, F_3$: PW1,DF1
100%	Gain Flatness versus Frequency	dG	0	2	dB	$V_{DD}=V_1$; $I_{DQ}=I_{DQ1}$; $T_F=T_{F1}$; $P_O=P_{OUT1}$; $F=F_1, F_2, F_3$: PW1,DF1
100%	Drain Efficiency	Nd	38	75	%	$V_{DD}=V_1$; $I_{DQ}=I_{DQ1}$; $T_F=T_{F1}$; $P_O=P_{OUT1}$; $F=F_1, F_2, F_3$: PW1,DF1
100%	Stability into 1.5:1 VSWR	VSWR-S	S	--	--	$V_{DD}=V_1$; $I_{DQ}=I_{DQ1}$; $T_F=T_{F1}$; $P_O=P_{OUT1}$; $F=F_1, F_2, F_3$: PW1,DF1 Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	2:1 Load Mismatch Tolerance	LMT	P	--	--	$V_{DD}=V_1$; $I_{DQ}=I_{DQ1}$; $T_F=T_{F1}$; $P_i = P_{IN1}$; $F=F_1, F_2, F_3$: PW1,DF1 Rotate 2:1 output VSWR through 360° phase.
Note 1	$V_1=28V$; I_{DQ1} (Drain Quiescent Current)=40mA/side; PW1(Pulse Width 1) =0.5ms; DF1(Duty Factor 1)=17%; $P_{IN1}=24W$.					
Note 2	Test Frequencies: $F_1=2.25GHz$, $F_2=2.4GHz$, $F_3=2.55GHz$.					
Note 3	$T_{F1}=30\pm5^\circ C$ = Device Flange Temperature.					
Note 4	RF Electrical characteristics tested in broadband RF test fixture.					

BROADBAND RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
2.25	TBD	TBD
2.40	TBD	TBD
2.55	TBD	TBD

Z_{IF} = The test fixture input impedance for each side.

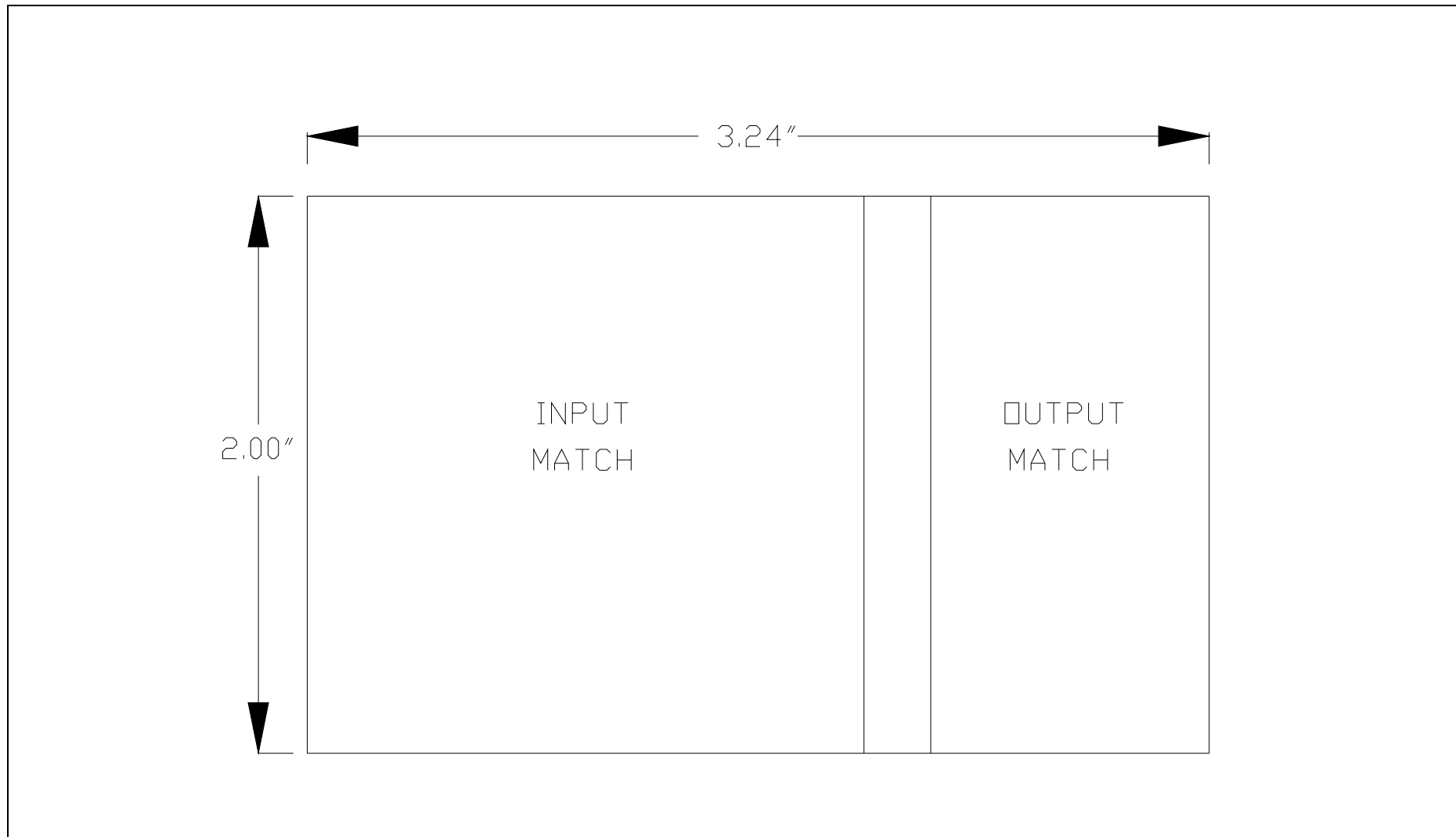
Z_{OF} = The test fixture output impedance for each side.

PACKAGE DIMENSIONAL OUTLINE DRAWING


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.27
B	1.395	1.405	35.43	35.69
C	0.634	0.674	16.10	17.12
D	0.395	0.405	10.03	10.29
E	1.219	1.241	30.96	31.52
F	0.455	0.465	11.56	11.81
G	0.075	0.085	1.90	2.16
H	0.120	0.130	3.05	3.30
J	0.535	0.545	13.59	13.84
K	0.059	0.069	1.499	1.753
L	0.081	0.091	2.06	2.31
M	0.164	0.194	4.16	4.93
N	0.004	0.007	0.10	0.18
□	0.354	0.364	8.99	9.24

PIN SCHEDULE	
1	SOURCE
2	GATE
3	DRAIN

RF-TEST-FIXTURE



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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