Part Number: ILD2735M120 (Preliminary)

Integra
TECHNOLOGIES, INC.

S-Band Radar Transistor

Part number ILD2735M120 is designed for S-Band radar applications operating over the 2.7 – 3.5 GHz instantaneous frequency band. Under 300us / 10% pulsed conditions it supplies a minimum of 120 watts of peak output power. Specified operation is with Class AB bias. The broadband test fixture includes a temperature compensated bias network. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. This device is rated for a peak output power level of P_{PEAK} = 120W @ 10% duty factor. This corresponds to an average power P_{AVG} = 12W.

Silicon LDMOS FET
- – High Power Gain
- – Excellent thermal stability
- – Gold Metal

Gold Metal System
- – Complete Gold System
- – LDMOS with Gold Metal
- – Gold Bond Wires
- – Gold Package Metal
- – Maximum Reliability

Class AB Operation
- – Specified with AB bias

Internal Impedance Matching
- – Ease of Use
- – Ultra Low Loss Design

BeO Free Package
- – Metal Based
- – Epoxy Seal

High Power RF Test / Fixture
- – Broadband
- – Matched to 50 Ω (ohms)
- – Temperature Compensated Bias
- – Long-term Correlation
- – 100% Device RF Screening
- – No External Tuning required

GAIN VERSUS OUTPUT POWER

Part Number	FREQ (GHz)	Pin (W)	IRL (dB)	Pout (W)	Gp (dB)	ID (A)	Nd (%)	Droop (dB)
ILD2735M120-7 50020505-21	2.70	12.98	-18.00	120	9.66	11.56	32.4	-0.21
	2.90	11.38	-18.00	120	10.23	10.91	34.4	-0.18
	3.10	13.25	-17.63	120	9.57	11.28	33.2	-0.27
	3.30	11.73	-12.83	120	10.10	11.25	33.3	-0.28
	3.50	14.98	-11.61	120	9.04	10.83	34.6	-0.25

www.integratech.com
PHONE: 310-606-0855
FAX: 310-606-0865

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321 CORAL CIRCLE
EL SEGUNDO, CA 90245-4620

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
BD	CW Operation	--	--	--	--	Not rated for CW operation.
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.16	°C/W	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25±5°C, P_{OUT}=120W, N_D=28%
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	I_{DS}=10mA, V_{GS}=0V, T_F=25±5°C
BD	Drain Leakage Current	I_{DSS}	--	1.0	uA	V_{DS}=32V, V_{GS}=0V, T_F=25±5°C
100%	Operating Gate Voltage	V_{GS}	2.5	4.0	V	V_{DS}=32V, I_D=100mA, T_F=25±5°C
BD	Gate Leakage Current	I_{GSS}	--	1.0	uA	V_{GS}=10V, V_{DS}=0V, T_F=25±5°C

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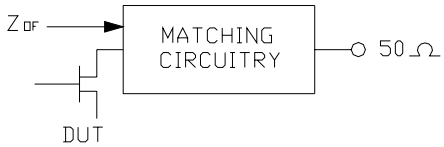
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-7	dB	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3, F4, F5.
100%	Input Power	P_{in}	11	17	W	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3, F4, F5
100%	Drain Efficiency	N_D	30	50	%	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3, F4, F5
100%	Pulse Amplitude Droop	D	-0.5	+0.5	dB	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3, F4, F5
100%	3:1 Load Mismatch Stability	VSWR-LMT	3:1	--	--	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3, F4, F5 Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least –65 dBc.
Note 1	V1 = 32V; I_{DQ1} = 60mA; PW1 = 300us; DF1 = 10%, P_{OUT1} = 120W.					
Note 2	Test Frequencies: F1 = 2.7 GHz, F2 = 2.9 GHz, F3 = 3.1 GHz, F4=3.3GHz, F5=3.5GHz					
Note 3	T_{F1} = 25±5°C = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					
Note 5	Phase Marking -1 thru -12 for 5° phase; variation between -30° to +30° measured at 3.5GHz.					

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	Z_{IF} (Ω) /Side	Z_{OF} (Ω) /Side
2.70	2.10 – j 5.50	5.0 – j 5.0
2.90	2.50 – j 4.00	4.7 – j 4.0
3.10	2.8 – j 2.70	4.5 – j 3.1
3.30	3.1 – j 1.30	4.2 – j 2.0
3.50	3.3 – j 0.10	3.8 – j 1.1
Impedance Definition		

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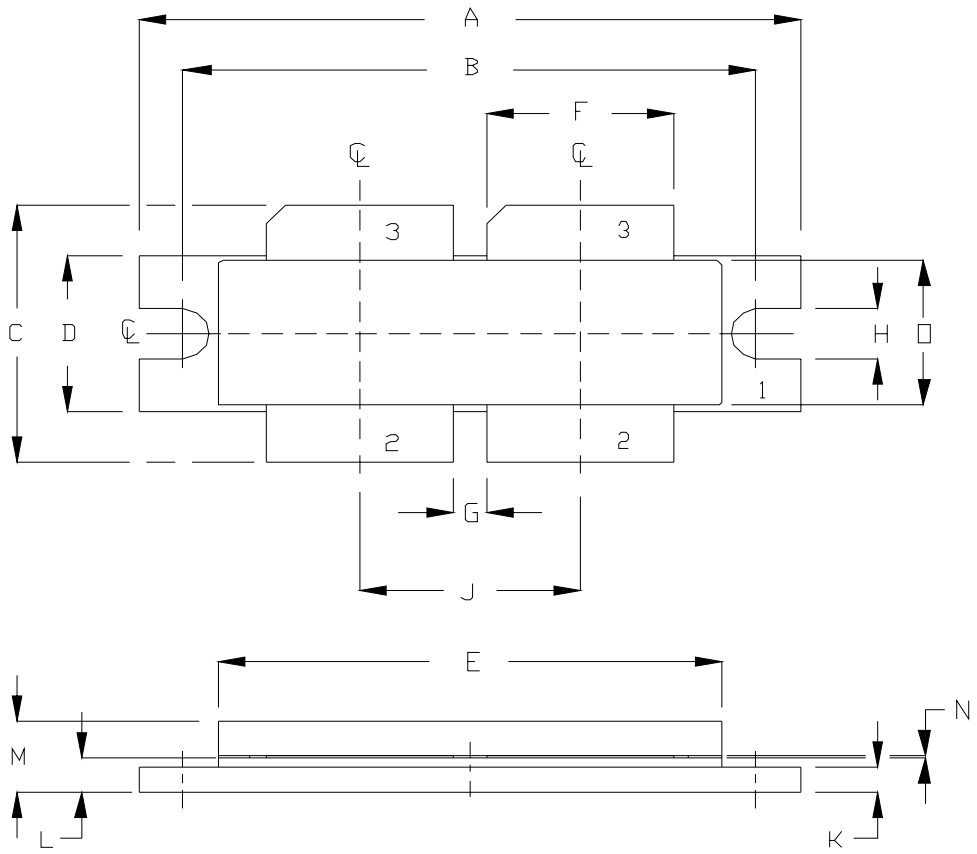
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.27
B	1.395	1.405	35.43	35.69
C	0.634	0.674	16.10	17.12
D	0.395	0.405	10.03	10.29
E	1.219	1.241	30.96	31.52
F	0.455	0.465	11.56	11.81
G	0.075	0.085	1.90	2.16
H	0.120	0.130	3.05	3.30
J	0.535	0.545	13.59	13.84
K	0.059	0.069	1.499	1.753
L	0.081	0.091	2.06	2.31
M	0.164	0.194	4.16	4.93
N	0.004	0.007	0.10	0.18
□	0.354	0.364	8.99	9.24

PIN SCHEDULE	
1	SOURCE
2	GATE
3	DRAIN

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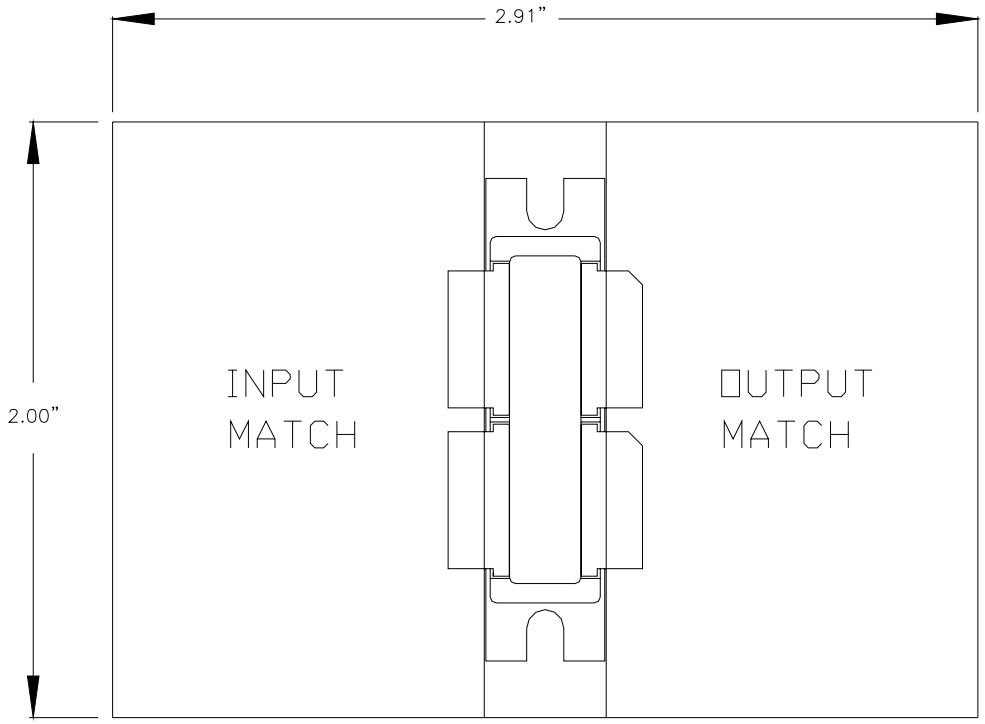
RF TEST FIXTURE – ASSEMBLY AND PARTS LIST



CONTACT FACTORY FOR DETAILED RF TEST FIXTURE CAD DRAWING

www.integratech.com
PHONE: 310-606-0855
FAX: 310-606-0865

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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.

Maximum Ratings
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

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