

## S-Band Radar Transistor

Part number ILD3135M30 is designed for S-Band radar applications operating over the 3.1 – 3.5 GHz instantaneous frequency band. Under 300us / 10% pulse conditions it supplies a minimum of 30 watts of peak output power with 10dB gain typically. Specified operation is with Class AB bias. The device also may be operated with Class A or B bias. When appropriately rated, it is operable under a wide range of pulse widths and duty factors. It operates with spectral purity into all phases of 3:1 output load VSWR. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening.



### Silicon LDMOS FET

- High Power Gain
- Excellent thermal stability
- Gold Metal

### Gold Metal System

- Complete Gold System
- LDMOS with Gold Metal
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

### Class A, AB, B Operation

- Specified with AB bias
- Operable with A bias
- Operable with B bias

### Internal Impedance Matching

- Ease of Use
- Ultra Low Loss Design

### BeO Free Package

- Metal Based
- Epoxy Seal

### High Power RF Test / Fixture

- Broadband
- Matched to 50  $\Omega$  (ohms)
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

## TYPICAL DATA      TYPICAL DATA      TYPICAL DATA      TYPICAL DATA

FREQ (GHz)	V <sub>dd</sub> (V)	P <sub>IN</sub> (W)	IRL (dB)	P <sub>OUT</sub> (W)	G <sub>P</sub> (dB)	I <sub>D</sub> (A)	OPF (dB)	Droop (dB)	VSWR-S 3:1	VSWR-S 3:1
3.100	32.0	3.50	-18.00	38.15	10.37	3.14	0.09	-0.26	S	P
3.300	32.0	3.50	-12.57	38.13	10.37	3.30		-0.34	S	P
3.500	32.0	3.50	-11.55	38.93	10.46	3.00		-0.22	S	P

Pulse Format = 300us, 10%

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	$V_{DS}$	--	65	V	--
BD	Gate-Source Voltage	$V_{GS}$	-0.5	12	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	1.2	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=30W$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

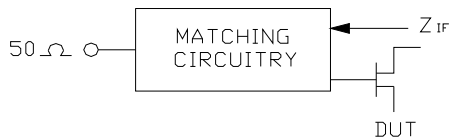

**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	$BV_{DSS}$	65	--	V	$I_{DS}=10mA, V_{GS}=0V, T_F=25\pm5^\circ C$
BD	Drain Leakage Current	$I_{DSS}$	--	1.0	uA	$V_{DS}=32V, V_{GS}=0V, T_F=25\pm5^\circ C$
100%	Operating Gate Voltage	$V_{GS}$	2.5	4.0	V	$V_{DS}=32V, I_D=0.1A, T_F=25\pm5^\circ C$
BD	Gate Leakage Current	$I_{GSS}$	--	1.0	uA	$V_{GS}=10V, V_{DS}=0V, T_F=25\pm5^\circ C$

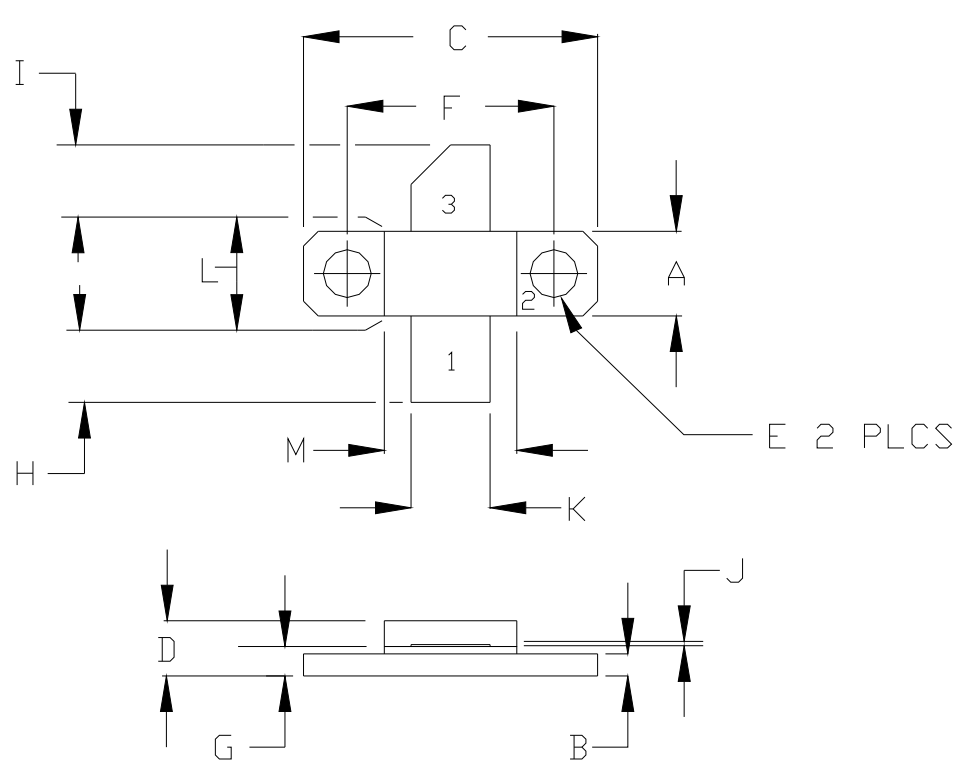
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-7	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power	$P_O$	30	50	W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Current – Peak	$I_D$	2.0	5.0	A	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	Droop	-0.3	0.3	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Power Gain	$G_p$	9.3	11.5	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	3:1 Load Mismatch Stability	VSWR-S	S	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$ Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
100%	Output Power Flatness (10 Log ( $P_{OUT Max}/P_{OUT Min}$ ))	OPF	0	1	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
Note 1	$V1 = 32V; I_{DQ1} = 10mA; PW1 = 300us; DF1 = 10%$					
Note 2	Input Power Test Levels: $P_{IN1} = 3.5W$					
Note 3	Test Frequencies: $F1 = 3.1 GHz, F2 = 3.3 GHz, F3 = 3.5 GHz.$					
Note 4	$T_{F1} = 25\pm5^\circ C =$ Device flange temperature.					
Note 5	Screen 'BD' = parameter qualified By Design.					

**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (GHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
3.10	2.9 – j5.5	4.2 – j10.0
3.30	2.7 – j4.7	3.8 – j9.2
3.50	2.6 – j3.9	3.5 – j8.4
Impedance Definition		

**PACKAGE DIMENSIONAL OUTLINE DRAWING**

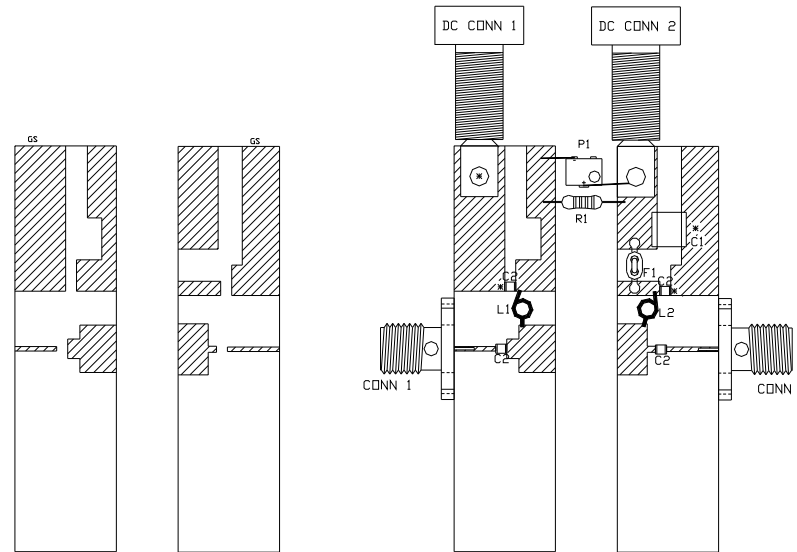


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.077	0.087	1.95	2.20
H	0.215	0.245	5.46	6.22
I	0.215	0.245	5.46	6.22
J	0.004	0.006	0.10	0.15
K	0.210	0.220	5.33	5.58
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN SCHEDULE	
1	GATE
2	SOURCE
3	DRAIN

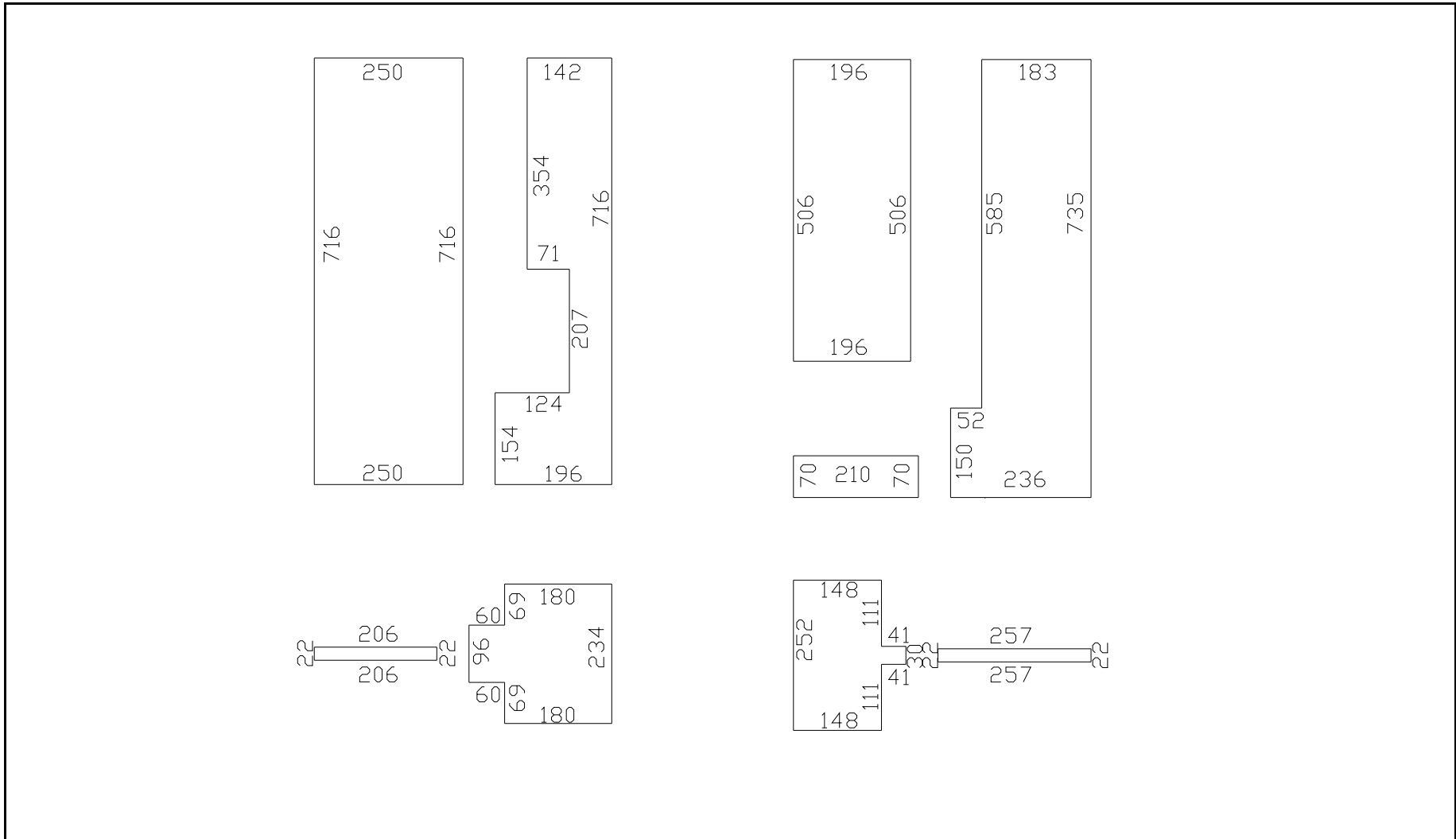
NOTES:  
LID: LID-PL32-1

**RF TEST FIXTURE – ASSEMBLY AND PARTS LIST**

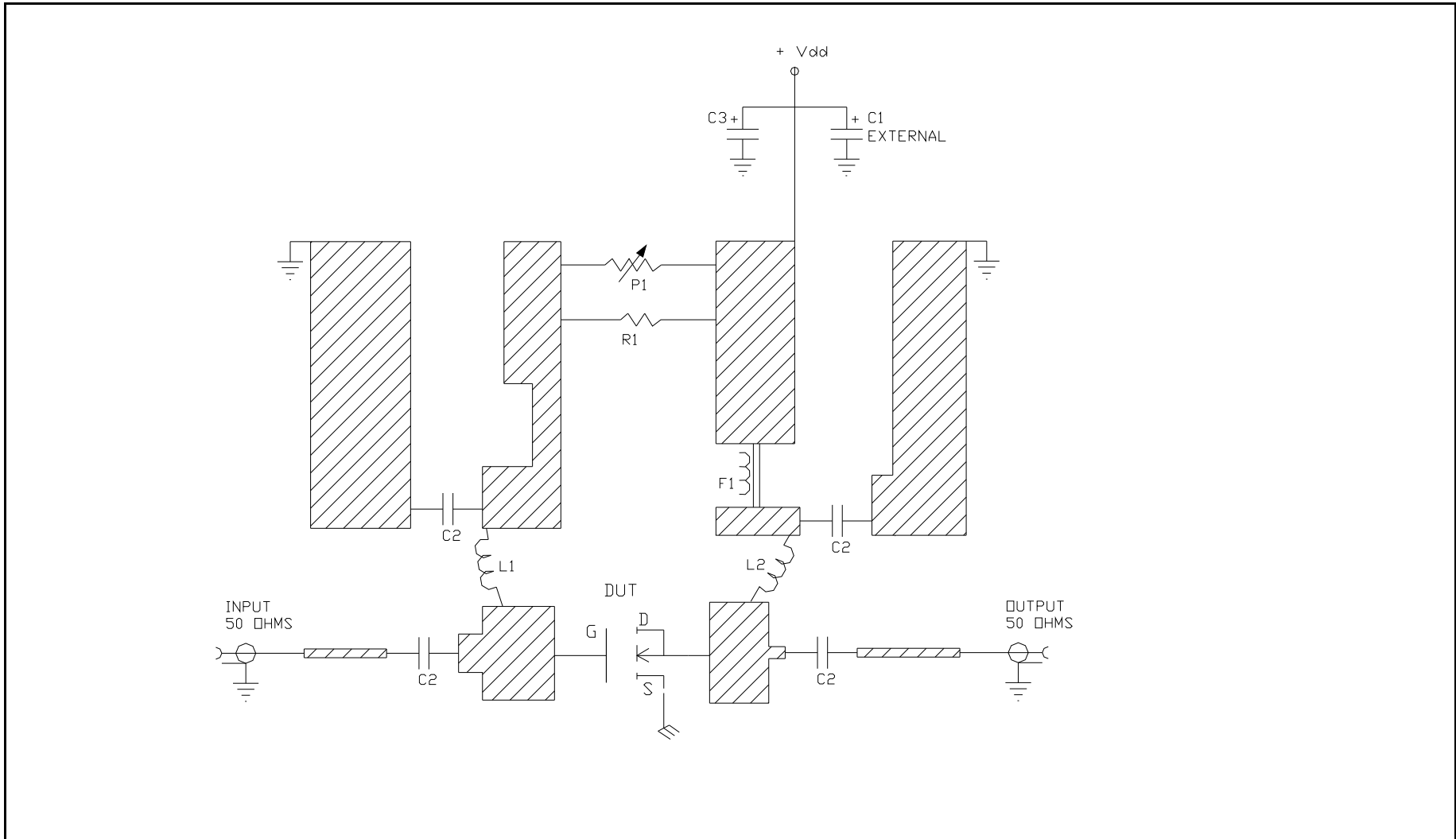


COMPONENT	DESCRIPTION
DUT	TRANSISTOR #ILD3135M30 MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #R06010.2 10z Cu 25 MILS THICK
C1, C3	ELECTROLYTIC CAPACITOR 4.7uF/50V
C2	CHIP CAPACITOR TYPE ARC100A 39pF
L1, L2	COIL: 4 TURN AWG#22 INSULATED, .076" DIA PULL TIGHT FULLY CLOSED, LEFT HAND.
F1	FERRITE TWIN HOLE CORE, 1 TURN AWG# 22 INSULATED
R1	RESISTOR 12K OHMS
P1	POTENTIOMETER
GS (5 PLACES)	GROUND SHIM, COPPER, TH=0.001"
CONN 1, CONN 2	SMA CONNECTOR, DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-01 (0.50")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-01 (0.50")
TRANSISTOR CARRIER	2 INCH COPPER-01(P32)
TRANSISTOR CLAMP	NDRYL CLAMP-01 (P32)
ALUMINUM HEAT SINK	2 INCH HEATSINK-09
DC CONN 1	BANANA JACK, BLACK
DC CONN 2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

**RF TEST FIXTURE – CIRCUIT DIMENSIONS IN MILS**



**RF TEST FIXTURE – ELECTRICAL SCHEMATIC**



**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

**WARNING**

<b>Product and environmental safety - toxic materials</b>
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

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