

S-Band Radar Miniature Power Amplifier

Part number MPAL2731M130 is a miniaturized power amplifier which is internally matched to 50 ohms. It is designed for S-Band radar systems and operates over the instantaneous bandwidth of 2.7-3.1 GHz. It utilizes gold metal LDMOS transistor technology operating in common source configuration. It may be operated in class B, AB and A mode. It is operable over nearly any pulse width and duty factor. Under 100us / 10% pulsed operation it can be used to supply a minimum of 130 watts of peak pulse power over the instantaneous frequency range of 2.7-3.1 GHz. All devices are 100% screened for large signal RF parameters.



50 Ohm Matched

- Requires no external impedance matching circuitry

Silicon LDMOS Transistor

- Gold Metal
- Excellent thermal stability

Class AB Operation

- Internal 1K Gate to ground resistor for ease of biasing

Common Source Configuration

- Linear Transfer Characteristic

Gold Metal System

- Complete Gold System
- LDMOS with Gold Metal
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

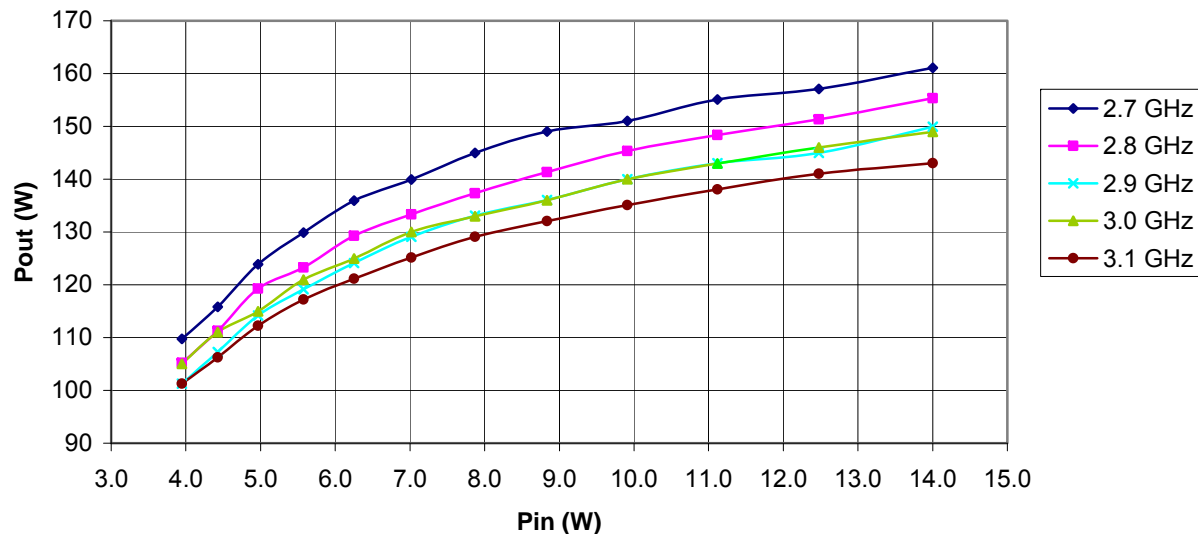
BeO Package

- Epoxy seal

RF High Power Test

- 100% Device RF High Power Screening in 50Ω Fixture
- No Circuit Tuning Required
- Long-term Correlation Maintained

Input Power versus Output Power



MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.19	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F1.$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

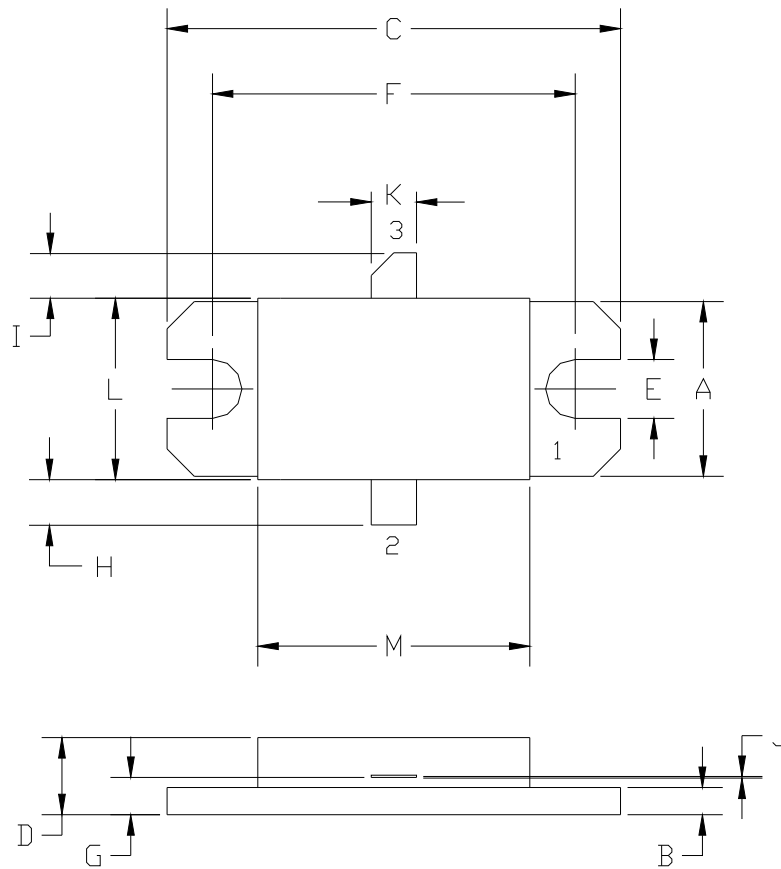
DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	$I_{DS} = 10mA, V_{GS} = 0V, T_F = 25\pm5^\circ C.$
BD	Drain Leakage Current	I_{DSS}	--	1.0	μA	$V_{DS} = 28V, V_{GS} = 0V, T_F = 25\pm5^\circ C.$
100%	Operating Gate Voltage	V_{GS}	2.5	4.0	V	$V_{DS} = 5V, I_D = 0.1A, T_F = 25\pm5^\circ C.$
BD	Gate Leakage Current	I_{GSS}	--	1.0	μA	$V_{GS} = 10V, V_{DS} = 0V, T_F = 25\pm5^\circ C.$

RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Input Return Loss	IRL1	-18	-10	-7	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F1.$
100%	Input Return Loss	IRL2	-18	-12	-8	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F2.$
100%	Input Return Loss	IRL3	-18	-16	-9	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F3.$
100%	Input Return Loss	IRL4	-18	-13	-10	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F4.$
100%	Input Return Loss	IRL5	-18	-12	-10	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F5.$
100%	Output Power	P _{out}	130	155	180	W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5.$
100%	Power Gain	G _P	10.0	11.0	12.0	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5.$
100%	Power Gain Flatness versus Frequency	GF	0.0	0.5	1.0	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5.$
100%	Drain Current - Peak	I _D	8.9	10.5	12.0	A	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5.$
100%	Pulse Amplitude Droop	D	-0.50	-0.20	+0.20	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5.$
100%	Stability into 2:1 VSWR	VSWR-S		--	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F1, F2, F3, F4, F5.$ Rotate 2:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
Note 1	V1 = 32V; I _{DQ1} = 50mA; PW1 = 100μs; DF1 = 10%						
Note 2	P _{IN1} = 14W						
Note 3	Test Frequencies: F1 = 2.70 GHz, F2 = 2.80 GHz, F3 = 2.90 GHz, F4 = 3.00 GHz, F5 = 3.10 GHz						
Note 4	T _F = 25±5°C = Device Flange Temperature						

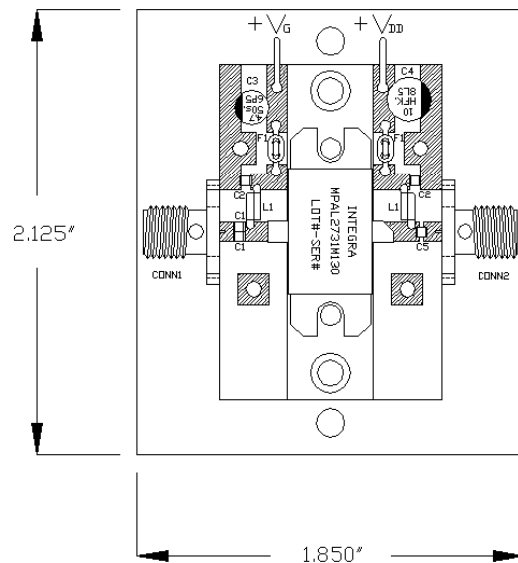
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.380	0.390	9.65	9.91
B	0.043	0.053	1.09	1.35
C	0.905	1.005	22.99	25.53
D	0.178	0.188	4.52	4.78
E	0.125	0.135	3.18	3.43
F	0.795	0.805	20.19	20.45
G	0.082	0.092	2.08	2.34
H	0.095	0.105	2.41	2.67
I	0.095	0.105	2.41	2.67
J	0.002	0.004	0.05	0.10
K	0.095	0.105	2.41	2.67
L	0.395	0.405	10.03	10.29
M	0.595	0.605	15.11	15.37

PIN SCHEDULE	
1	SOURCE-GROUND
2	GATE-INPUT
3	DRAIN-OUTPUT

RF TEST FIXTURE



COMPONENT	DESCRIPTION
DUT	DUT, MOUNT HARD TO THE RIGHT, NO CLAMP
PC BOARD	ROGERS# 5880, TH=0.031" 1E/1E
C1	CHIP CAPACITOR, TYPE ATC100A, 10 pF
C2	CHIP CAPACITOR, TYPE ATC100A, 20 pF
C3	ELECTROLYTIC CAPACITOR, 4.7uF / 50V DIGI-KEY PN# PCE3817CT-ND, PANASONIC# EEE-FK1H4R7R
C4	ELECTROLYTIC CAPACITOR, 10uF / 50V DIGI-KEY PN# PCE3808CT-ND, PANASONIC# EEE-1H100UR
C5	CHIP CAPACITOR, TYPE ATC100A, 12 pF
R1	POTENTIOMETER 1/4" 100kohms 10%, MOUSER P/N: 652-3266W-1-104LF, MFG P/N: 3266W-1-104LF
R2	AXIAL RESISTOR, 10K OHMS, 1/4W
L1	COIL: 2 TURN AWG# 22 INSULATED, ID 0.0625" DIA, PULL TIGHT AND FULLY CLOSED, LEFT HAND.
L2	COIL: 2 TURN AWG# 22 INSULATED, ID 0.0625" DIA, PULL TIGHT AND FULLY CLOSED, RIGHT HAND.
F1	FERRITE TWIN HOLE CORE, FERRONICS PN# 12-315-J, 1 TURN AWG# 22 INSULATED.
GS	GROUND SHIM, COPPER, TH=0.001"
CONN1, CONN2	SMA CONNECTOR, TYPE QS# 2052-5636-02
HEATSINK	2 INCH HEATSINK - 09
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

L:/Public/Controlled Documents/Controlled Drawings/RF Test Fixture Drawings/MPAL2731M130 REV NC.dwg

ASSEMBLY AND PARTS LIST

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

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